ภาคผนวก

MOTOROLA

MC34060A
MC33060A

Precision SWITCHMODE™ Pulse Width Modulator Control Circuit

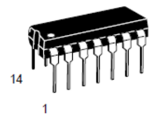
The MC34060A is a low cost fixed frequency, pulse width modulation control circuit designed primarily for single–ended SWITCHMODE power supply control.

The MC34060A is specified over the commercial operating temperature range of 0° to +70°C, and the MC33060A is specified over an automotive temperature range of –40° to +85°C.

- Complete Pulse Width Modulation Control Circuitry
- On–Chip Oscillator with Master or Slave Operation
- On–Chip Error Amplifiers
- On–Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Dead–Time Control
- Uncommitted Output Transistor Rated to 200 mA Source or Sink
- Undervoltage Lockout

PRECISION SWITCHMODE PULSE WIDTH MODULATOR CONTROL CIRCUIT

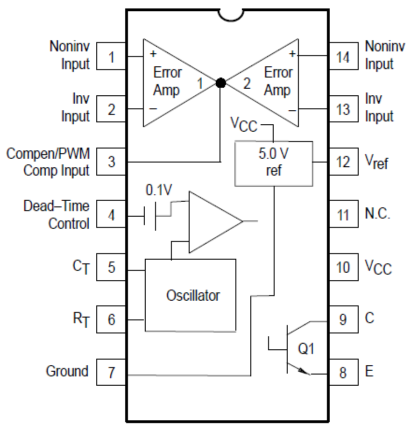
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34060AD	T_A = 0° to +70°C	SO–14
MC34060AP		Plastic DIP
MC33060AD	T_A = – 40° to +85°C	SO–14
MC33060AP		Plastic DIP

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	42	V
Collector Output Voltage	V_C	42	V
Collector Output Current (Note 1)	I_C	500	mA
Amplifier Input Voltage Range	V_{in}	–0.3 to +42	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	mW
Operating Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Operating Ambient Temperature Range For MC34060A For MC33060A	T_A	 0 to +70 –40 to +85	°C

NOTES: 1. Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristics	Symbol	P Suffix Package	D Suffix Package	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	80	120	°C/W
Derating Ambient Temperature	T_A	45	45	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	–	30	40	V
Collector Output Current	I_C	–	–	200	mA
Amplifier Input Voltage	V_{in}	–0.3	–	V_{CC} –2	V
Current Into Feedback Terminal	I_{fb}	–	–	0.3	mA
Reference Output Current	I_{ref}	–	–	10	mA
Timing Resistor	R_T	1.8	47	500	kΩ
Timing Capacitor	C_T	0.00047	0.001	10	µF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz
PWM Input Voltage (Pins 3 and 4)	–	–0.3	–	5.3	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA, T_A 25°C) $T_A = T_{low}$ to T_{high} – MC34060A – MC33060A	V_{ref}	4.925 4.9 4.85	5.0 – –	5.075 5.1 5.1	V
Line Regulation (V_{CC} = 7.0 V to 40 V, I_O = 10 mA))	Reg_{line}	–	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	2.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OUTPUT SECTION					
Collector Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	–	2.0	100	µA
Emitter Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V, V_E = 0 V)	$I_{E(off)}$	–	–	–100	µA
Collector–Emitter Saturation Voltage (Note 2)					V
Common–Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	–	1.1	1.5	
Emitter–Follower (V_C = 15 V, I_E = –200 mA)	$V_{sat(E)}$	–	1.5	2.5	
Output Voltage Rise Time (T_A = 25°C)	t_r				ns
Common–Emitter (See Figure 12)		–	100	200	
Emitter–Follower (See Figure 13)		–	100	200	
Output Voltage Fall Time (T_A = 25°C)	t_f				ns
Common–Emitter (See Figure 12		–	40	100	
Emitter–Follower (See Figure 13)		–	40	100	
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O[Pin\ 3]}$ = 2.5 V)	V_{IO}	–	2.0	10	mV
Input Offset Current ($V_{C[Pin\ 3]}$ = 2.5 V)	I_{IO}	–	5.0	250	nA
Input Bias current ($V_{O[Pin\ 3]}$ = 2.5 V)	I_{IB}	–	–0.1	–2.0	µA
Input Common Mode Voltage Range (V_{CC} = 40 V)	V_{ICR}	0 to V_{CC} –2.0	–	–	V
Inverting Input Voltage Range	$V_{IR(INV)}$	–0.3 to V_{CC}–2.0	–	–	V
Open–Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	–	dB
Unity–Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_c	–	600	–	kHz
Phase Margin at Unity–Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	–	65	–	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V, V_{in} = 0 V to 38 V))	CMRR	65	90	–	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	–	100	–	dB
Output Sink Current ($V_{O[Pin\ 3]}$ = 0.7 V)	I_{O-}	0.3	0.7	–	mA
Output Source Current ($V_{O[Pin\ 3]}$ = 3.5 V)	I_{O+}	–2.0	–4.0	–	mA

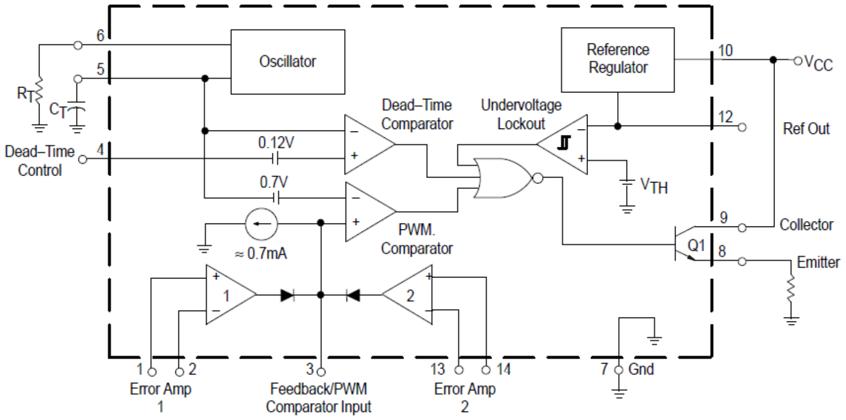
NOTES: 2. Low duty cycle techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.
T_{low} = –40°C for MC33060A T_{high} = +85°C for MC33060A
= 0°C for MC34060A = +70°Cfor MC34060A

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Test circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	3.5	4.5	V
Input Sink Current ($V_{[Pin\ 3]}$ = 0.7 V)	I_I	0.3	0.7	–	mA
DEAD–TIME CONTROL SECTION (Test circuit Figure 11)					
Input Bias Current (Pin 4) (V_{in} = 0 V to 5.25 V)	$I_{IB(DT)}$	–	–1.0	–10	µA
Maximum Output Duty Cycle (V_{in} = 0 V, C_T = 0.01 µF, R_T = 12 kΩ) (V_{in} = 0 V, C_T = 0.001 µF, R_T = 47 kΩ)	DC_{max}	 90 –	 96 92	 100 –	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 – 0	 2.8 –	 3.3 –	V
OSCILLATOR SECTION					
Frequency (C_T = 0.01 µF, R_T = 12 kΩ, T_A = 25°C) T_A = T_{low} to T_{high} – MC34060A – MC33060A (C_T = 0.001 µF, R_T = 47 kΩ)	f_{osc}	 9.7 9.5 9.0 –	 10.5 – – 25	 11.3 11.5 11.5 –	kHz
Standard Deviation of Frequency* (C_T = 0.001 µF, R_T = 47 kΩ)	σf_{osc}	–	1.5	–	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V)	$\Delta f_{osc}(\Delta V)$	–	0.5	2.0	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}) (C_T = 0.01 µF, R_T = 12 kΩ)	$\Delta f_{osc}(\Delta T)$	 – –	 4.0 –	 – –	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn–On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	4.0	4.7	5.5	V
Hysteresis	V_H	50	150	300	mV
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, all other inputs and outputs open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 – –	 5.5 7.0	 10 15	mA
Average Supply Current ($V_{[Pin\ 4]}$ = 2.0 V, C_T = 0.001 µF, R_T = 47 kΩ). See Figure 11.	I_S	–	7.0	–	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula; $\sigma = \sqrt{\frac{\sum_{n-1}^{N} (x_n - x)^2}{N-1}}$

Figure 1. Block Diagram



This device contains 46 active transistors.

Description

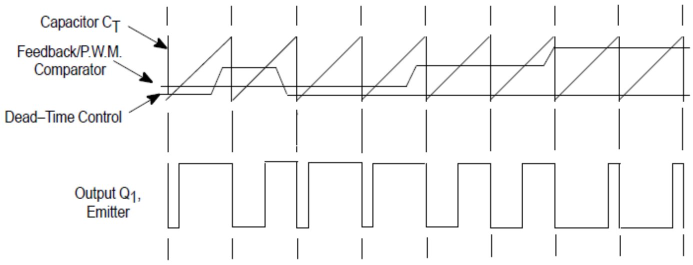
The MC34060A is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply (see Figure 1). An internal–linear sawtooth oscillator is frequency–programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.2}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control–signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

Figure 2. Timing Diagram



APPLICATIONS INFORMATION

The control signals are external inputs that can be fed into the dead–time control, the error amplifier inputs, or the feed–back input. The dead–time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth–cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time–control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on–time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from –0.3 V to (V_{CC} –2.0 V), and may be used to sense power supply output voltage and current. The error–amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC34060A has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of ±5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to +70°C.

Figure 3. Oscillator Frequency versus Timing Resistance

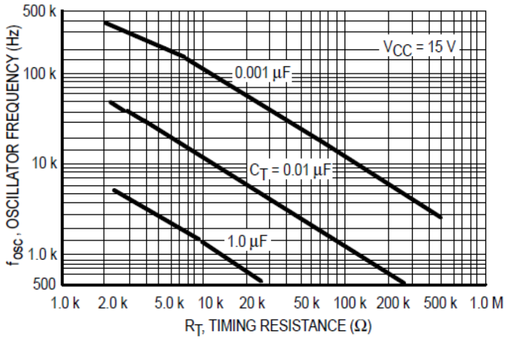


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

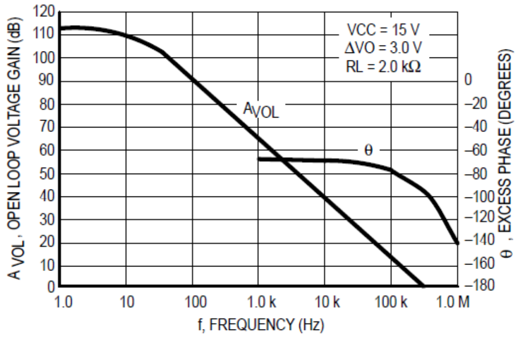


Figure 5. Percent Deadtime versus Oscillator Frequency

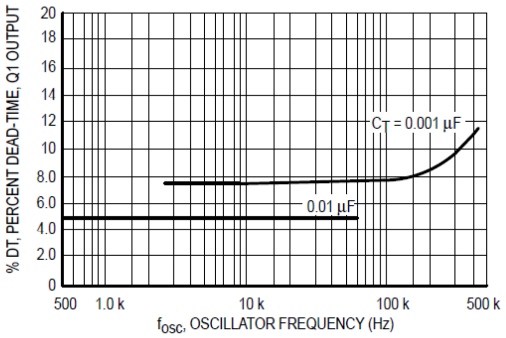


Figure 6. Percent Duty Cycle versus Dead–Time Control Voltage

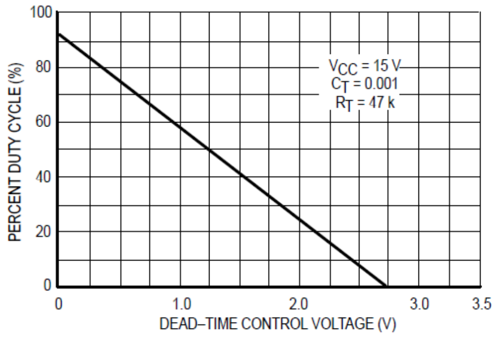


Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current

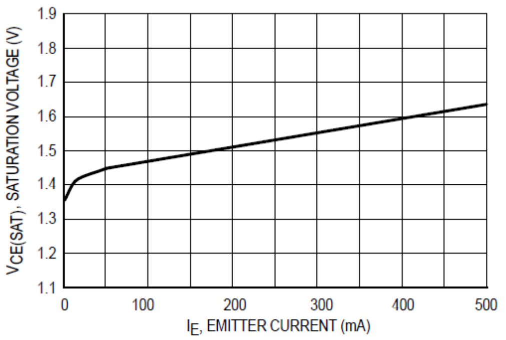


Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current

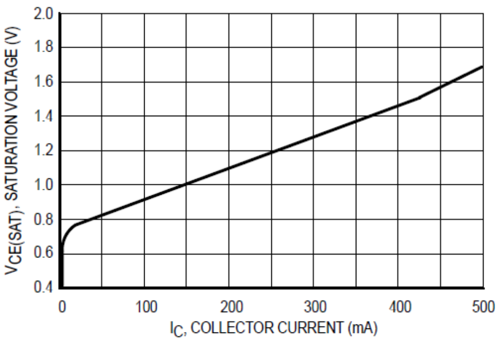


Figure 9. Standby Supply Current versus Supply Voltage

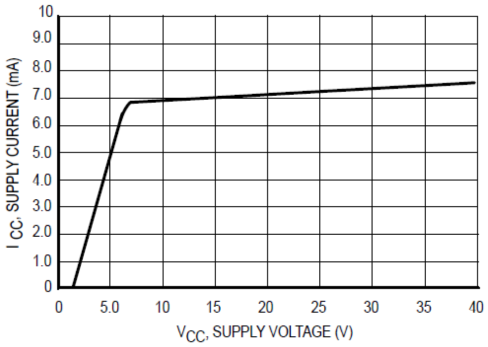


Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current

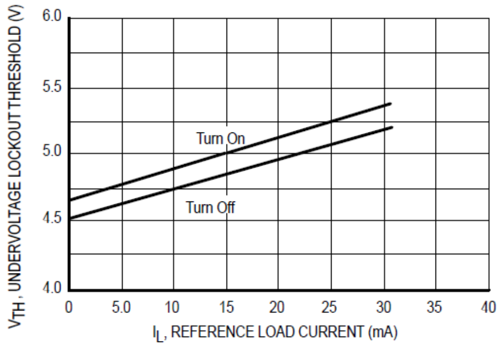


Figure 11. Error Amplifier Characteristics

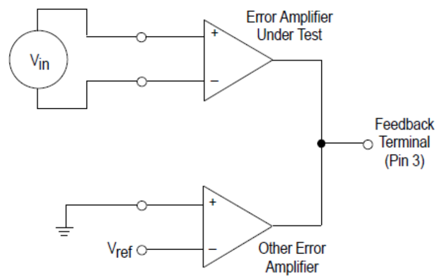


Figure 12. Deadtime and Feedback Control

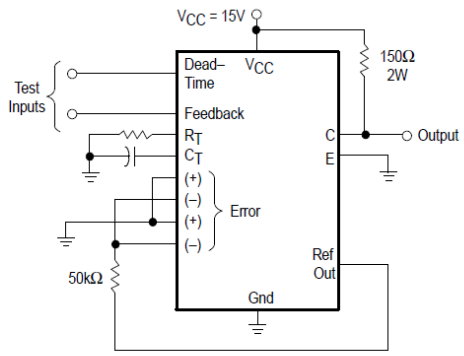


Figure 13. Common–Emitter Configuration and Waveform

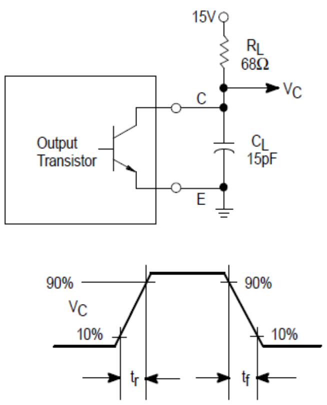
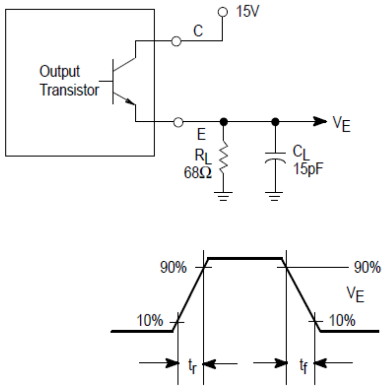


Figure 14. Emitter–Follower Configuration and Waveform



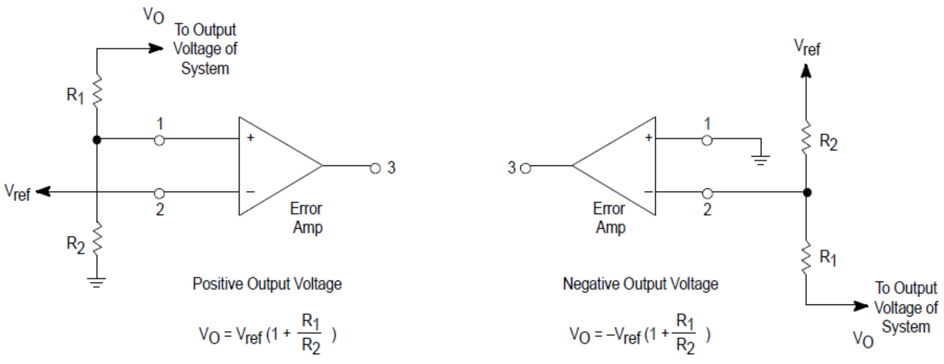


Figure 15. Error Amplifier Sensing Techniques

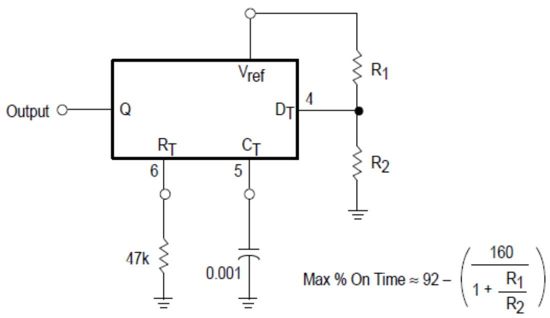


Figure 16. Deadtime Control Circuit

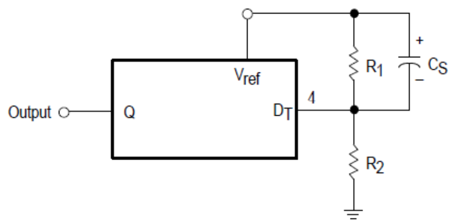


Figure 17. Soft–Start Circuit

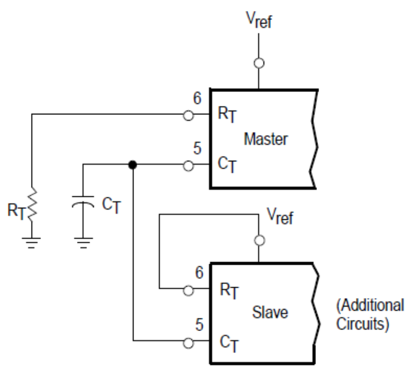
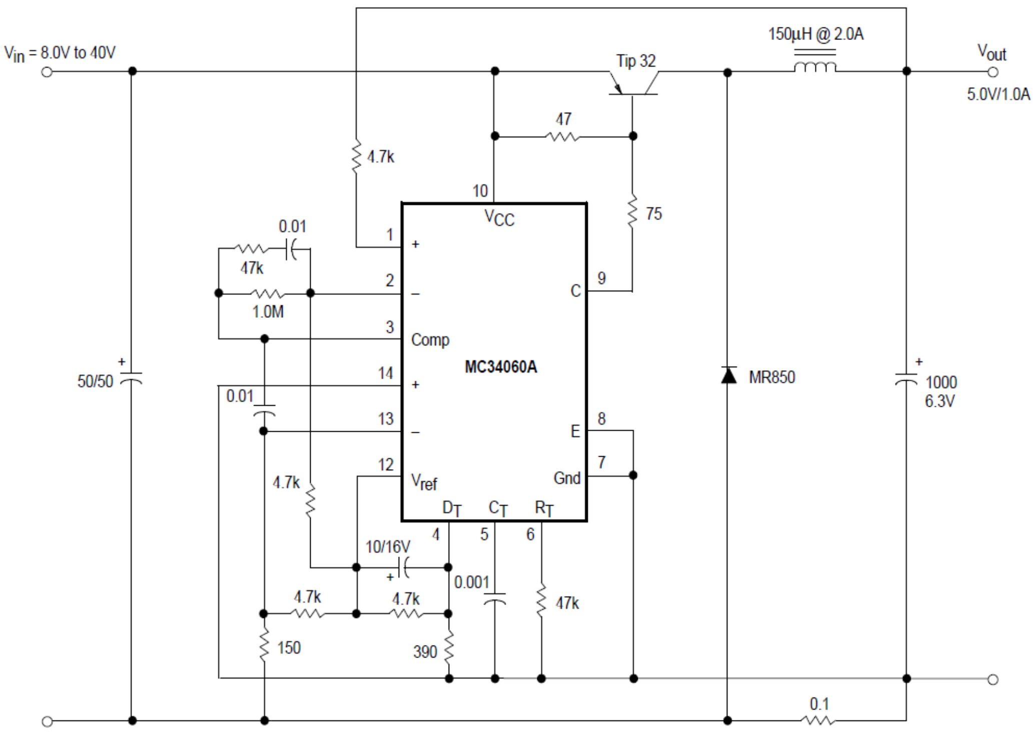


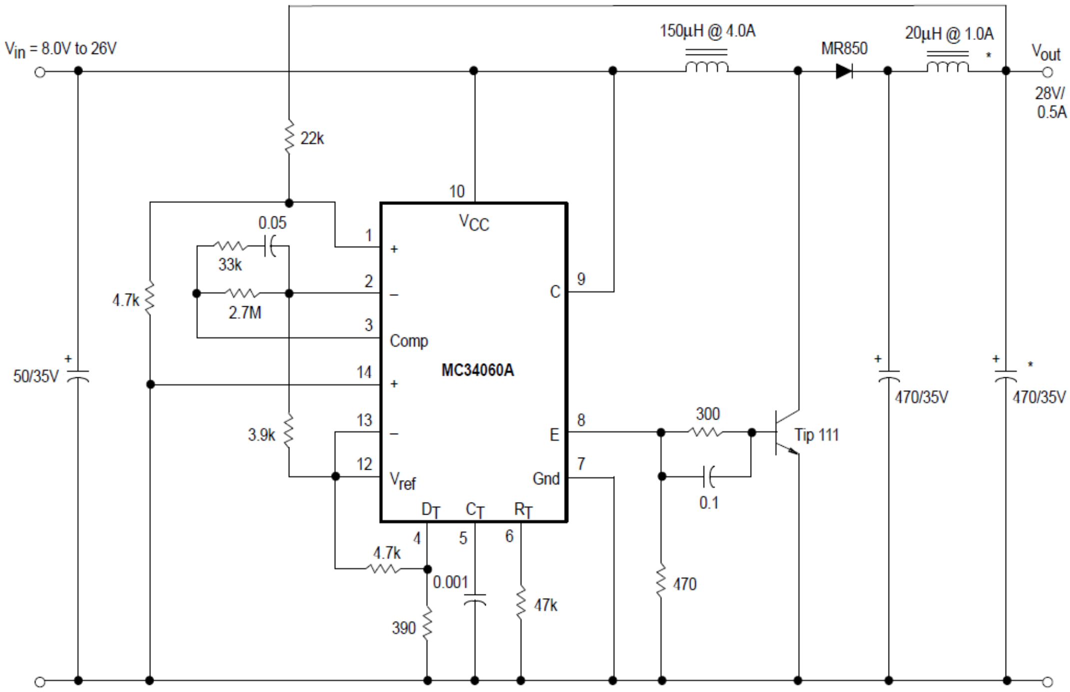
Figure 18. Slaving Two or More Control Circuits

Figure 19. Step–Down Converter with Soft–Start and Output Current Limiting



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 1.0 A	25 mV 0.5%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	75 mV p–p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	73%

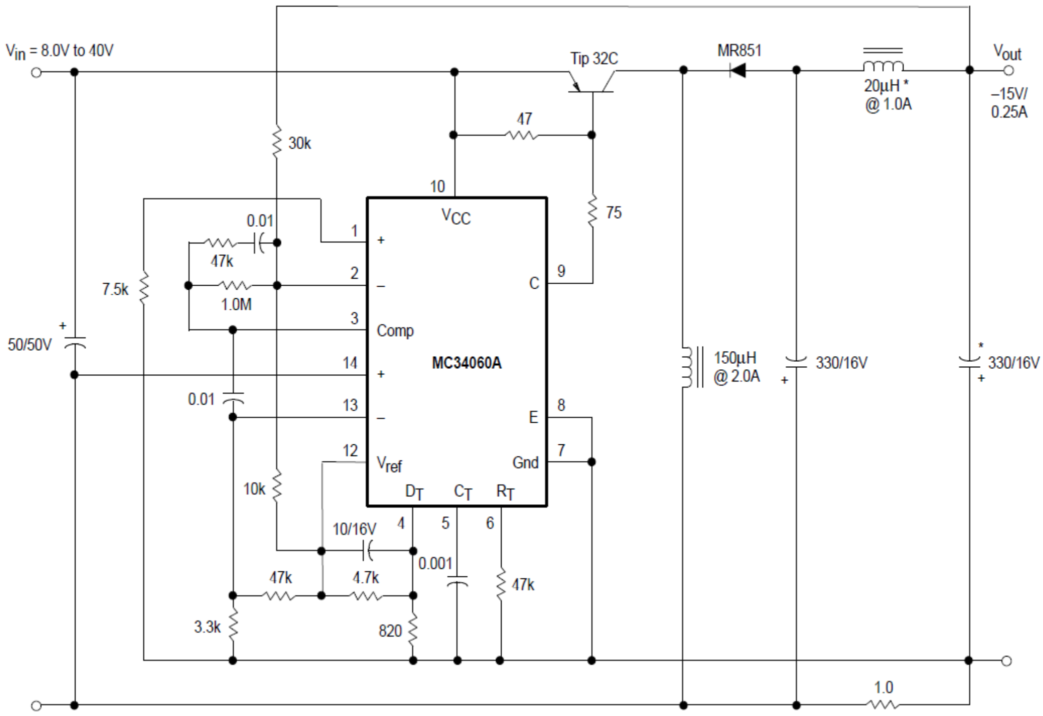
Figure 20. Step–Up Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 26 V, I_O = 0.5 A	40 mV 0.14%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 0.5 A	5.0 mV 0.18%
Output Ripple	V_{in} = 12 V, I_O = 0.5 A	24 mV p–p P.A.R.D.
Efficiency	V_{in} = 12 V, I_O = 0.5 A	75%

* Optional circuit to minimize output ripple

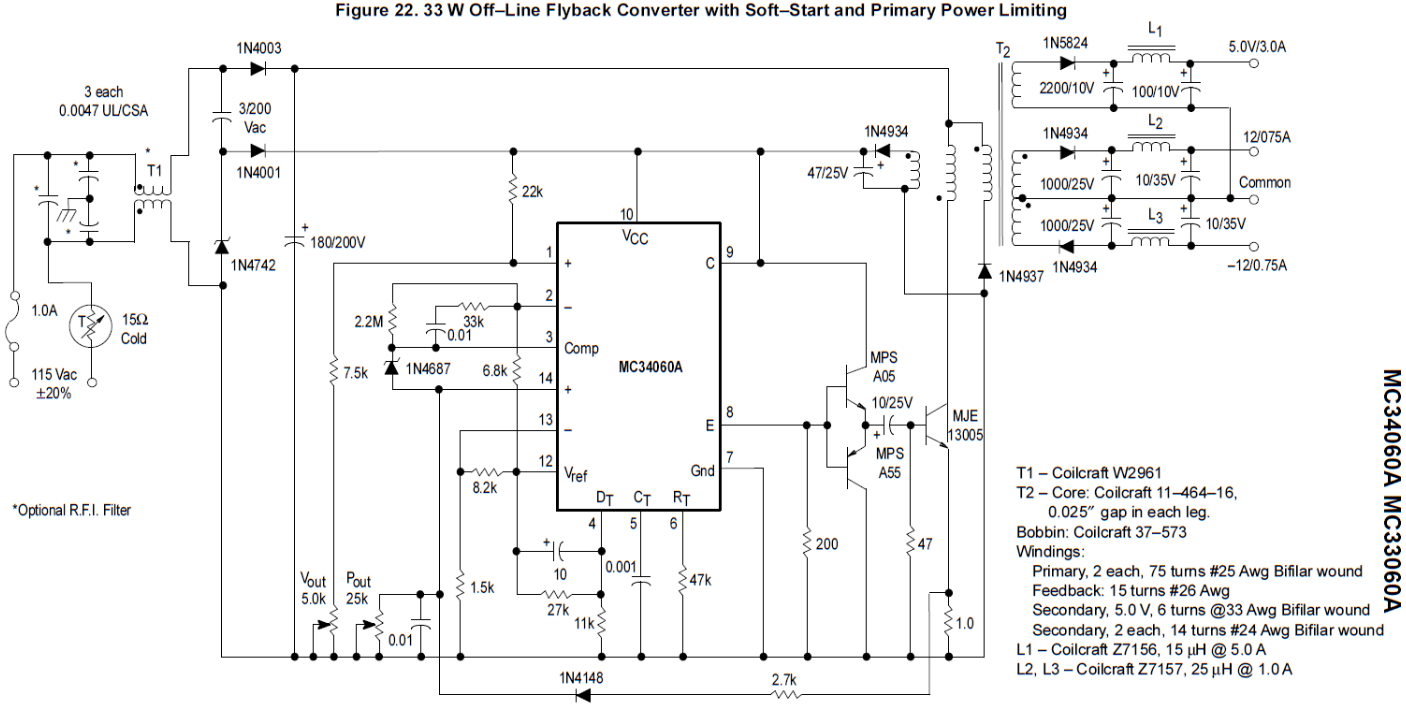
Figure 21. Step–Up/Down Voltage Inverting Converter with Soft–Start and Current Limiting



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 250 mA	52 mV 0.35%
Load Regulation	V_{in} = 12 V, I_O = 1.0 to 250 mA	47 mV 0.32%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	10 mV p–p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	330 mA
Efficiency	V_{in} = 12 V, I_O = 250 mA	86%

* Optional circuit to minimize output ripple

Figure 22. 33 W Off–Line Flyback Converter with Soft–Start and Primary Power Limiting

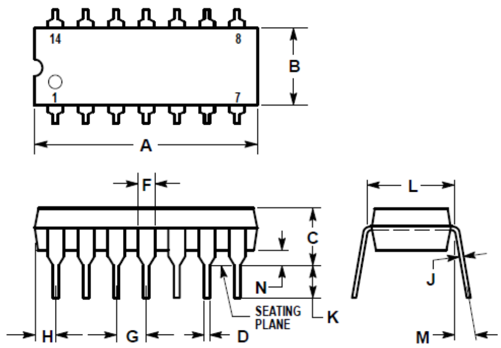


T1 – Coilcraft W2961
T2 – Core: Coilcraft 11–464–16,
0.025″ gap in each leg.
Bobbin: Coilcraft 37–573
Windings:
Primary, 2 each, 75 turns #25 Awg Bifilar wound
Feedback: 15 turns #26 Awg
Secondary, 5.0 V, 6 turns @33 Awg Bifilar wound
Secondary, 2 each, 14 turns #24 Awg Bifilar wound
L1 – Coilcraft Z7156, 15 µH @ 5.0 A
L2, L3 – Coilcraft Z7157, 25 µH @ 1.0 A

Test	Conditions	Results
Line Regulation 5.0 V	V_{in} = 95 Vac to 135 Vac, I_O = 3.0 A	20 mV 0.40%
Line Regulation ±12 V	V_{in} = 95 Vac to 135 Vac, I_O = ±0.75 A	52 mV 0.26%
Load Regulation 5.0 V	V_{in} = 115 Vac, I_O = 1.0 A to 4.0 A	476 mV 9.5%
Load Regulation ±12 V	V_{in} = 115 Vac, I_O = ±0.4 A to ±0.9 A	300 mV 2.5%
Output Ripple 5.0 V	V_{in} = 115 Vac, I_O = 3.0 A	45 mV p–p P.A.R.D.
Output Ripple ±12 V	V_{in} = 115 Vac, I_O = ±0.75 A	75 mV p–p P.A.R.D.
Efficiency	V_{in} = 115 Vac, I_O 5.0 V = 3.0 A I_O ±12 V = ±0.75 A	74%

OUTLINE DIMENSIONS

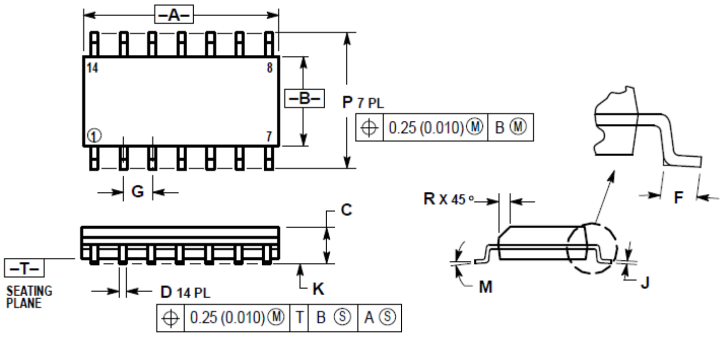
P SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
(SO–14)
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

FAIRCHILD
SEMICONDUCTOR™

October 1987
Revised January 1999

CD4049UBC • CD4050BC Hex Inverting Buffer • Hex Non-Inverting Buffer

General Description

The CD4049UBC and CD4050BC hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage (V_{DD}). The input signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at V_{DD} = 5.0V, they can drive directly two DTL/TTL loads over the full operating temperature range.

Features

- Wide supply voltage range: 3.0V to 15V
- Direct drive to 2 TTL loads at 5.0V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than V_{DD}

Applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS HIGH-to-LOW logic level converter

Ordering Code:

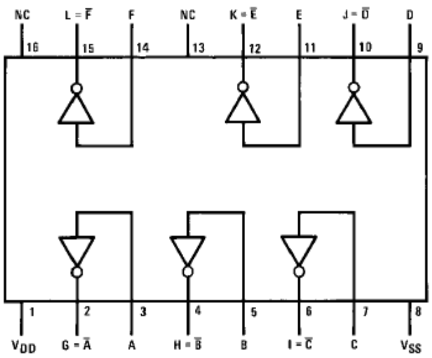
Order Number	Package Number	Package Description
CD4049UBCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4049UBCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4050BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4050BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

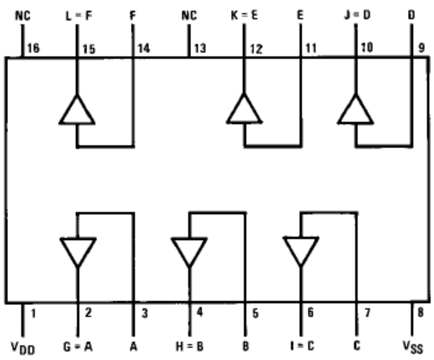
Pin Assignments for DIP

CD4049UBC



Top View

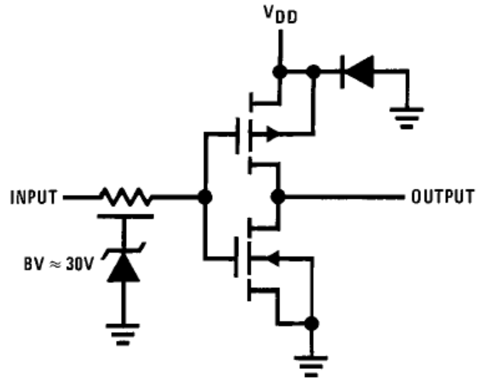
CD4050BC



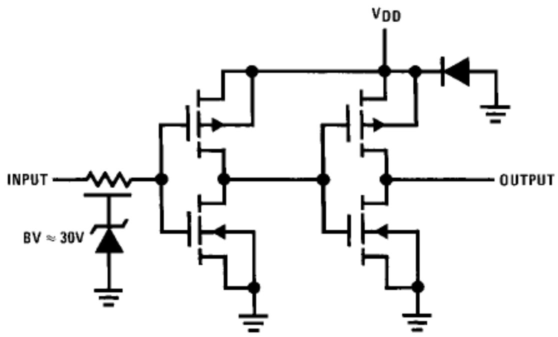
Top View

Schematic Diagrams

CD4049UBC
1 of 6 Identical Units



CD4050BC
1 of 6 Identical Units



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to +18V
Voltage at Any Output Pin (V_{OUT})	−0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to 15V
Voltage at Any Output Pin (V_{OUT})	0 to V_{DD}
Operating Temperature Range (T_A)	
CD4049UBC, CD4050BC	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4		0.03	4.0		30	µA
		V_{DD} = 10V		8		0.05	8.0		60	µA
		V_{DD} = 15V		16		0.07	16.0		120	µA
V_{OL}	LOW Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V,								
		$\|I_O\|$ < 1 µA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V,								
		$\|I_O\|$ < 1 µA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4050BC Only)	V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	V
V_{IL}	LOW Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4049UBC Only)	V_{DD} = 5V, V_O = 4.5V		1.0		1.5	1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0		2.5	2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0		3.5	3.0		3.0	V
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4050BC Only)	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4049UBC Only)	V_{DD} = 5V, V_O = 0.5V	4.0		4.0	3.5		4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0	7.5		8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0	11.5		12.0		V
I_{OL}	LOW Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
	(Note 4)	V_{DD} = 5V, V_O = 0.4V	4.6		4.0	5		3.2		mA
		V_{DD} = 10V, V_O = 0.5V	9.8		8.5	12		6.8		mA
		V_{DD} = 15V, V_O = 1.5V	29		25	40		20		mA
I_{OH}	HIGH Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
	(Note 4)	V_{DD} = 5V, V_O = 4.6V	−1.0		−0.9	−1.6		−0.72		mA
		V_{DD} = 10V, V_O = 9.5V	−2.1		−1.9	−3.6		−1.5		mA
		V_{DD} = 15V, V_O = 13.5V	−7.1		−6.2	−12		−5		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V	−0.3		−0.3	-10^{-5}			−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V	0.3		0.3	10^{-5}			1.0	µA

Note 3: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Continued)

Note 4: These are peak output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics (Note 5)

CD4049UBC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level	$V_{DD} = 5V$		30	65	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level	$V_{DD} = 5V$		45	85	ns
		$V_{DD} = 10V$		25	45	ns
		$V_{DD} = 15V$		20	35	ns
t_{THL}	Transition Time HIGH-to-LOW Level	$V_{DD} = 5V$		30	60	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{TLH}	Transition Time LOW-to-HIGH Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
C_{IN}	Input Capacitance	Any Input		15	22.5	pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

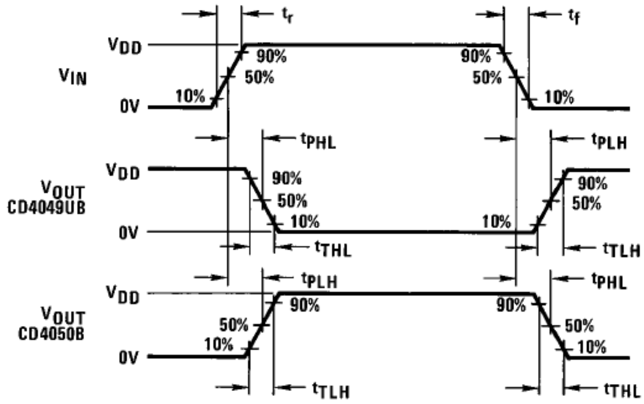
AC Electrical Characteristics (Note 6)

CD4050BC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

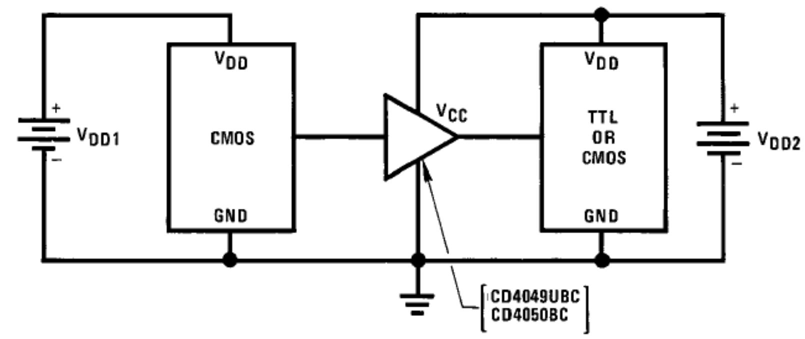
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level	$V_{DD} = 5V$		60	110	ns
		$V_{DD} = 10V$		25	55	ns
		$V_{DD} = 15V$		20	30	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
t_{THL}	Transition Time HIGH-to-LOW Level	$V_{DD} = 5V$		30	60	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{TLH}	Transition Time LOW-to-HIGH Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

Switching Time Waveforms



Typical Applications

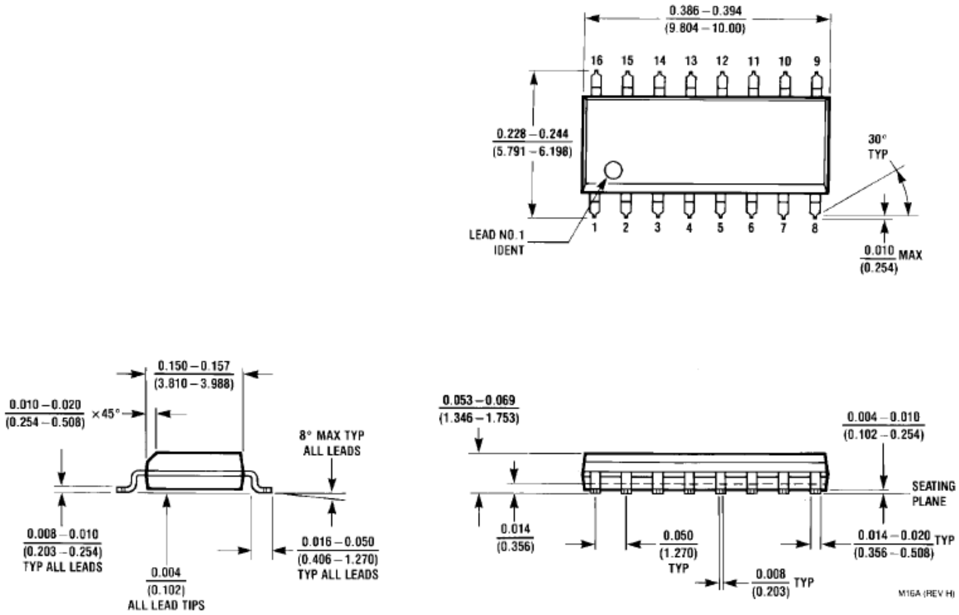
CMOS to TLL or CMOS at a Lower V_{DD}



$V_{DD1} \geq V_{DD2}$

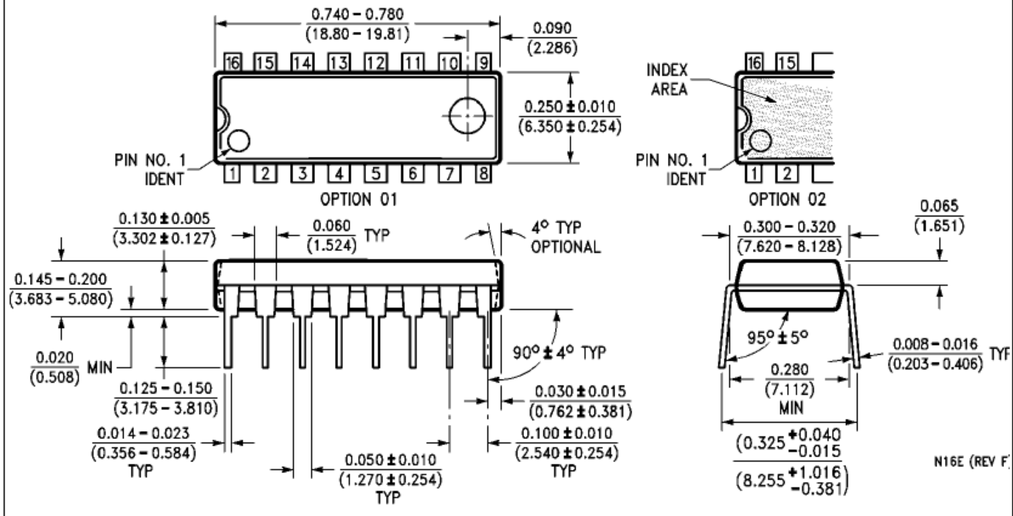
In the case of the CD4049UBC the output drive capability increases with increasing input voltage.
E.g., If V_{DD1} = 10V the CD4049UBC could drive 4 TTL loads.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



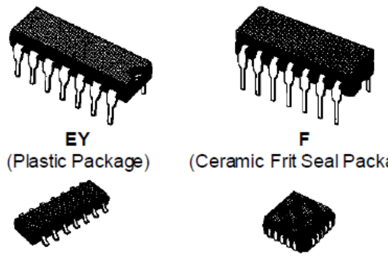
16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

HCC4073B/81B/82B
HCF4073B/81B/82B

AND GATES

4073B TRIPLE 3–INPUT AND GATE
4081B QUAD 2–INPUT AND GATE
4082B DUAL 4–INPUT AND GATE

- MEDIUM SPEED OPERATION – t_{PLH} = 85ns (typ.) ; t_{PHL} = 65ns (typ.) AT 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



EY (Plastic Package)
F (Ceramic Frit Seal Package)
M1 (Micro Package)
C1 (Plastic Chip Carrier)

ORDER CODES :

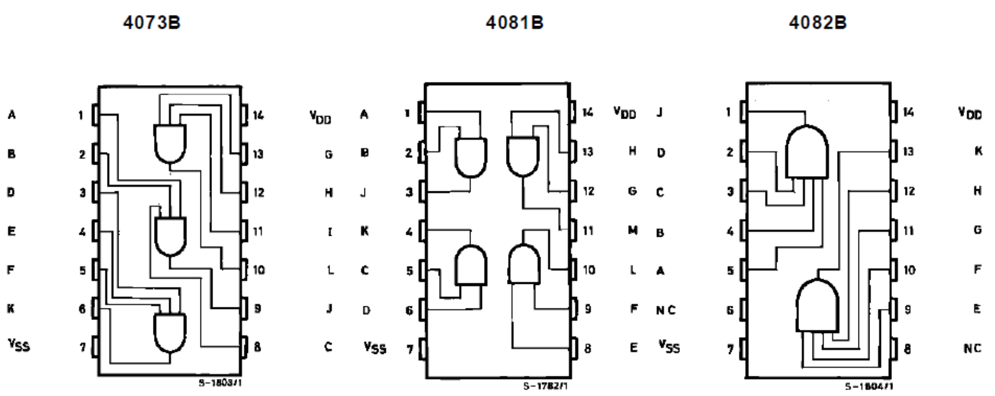
HCC40XXBF	HCF40XXBM1
HCF40XXBEY	HCF40XXBC1

DESCRIPTION

The **HCC4073B**, **HCC4081B** and **HCC4082B** (extended temperature range) and the **HCF4073B**, **HCF4081B** and **HCF4082B** (intermediate temperature range) are monolithic integrated circuits available in 14-lead dual in-line plastic or ceramic package and plastic micro package.

The **HCC/HCF4073B**, **4081B** and **4082B** AND gates provide the system designer with direct im-

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage : **HCC** Types **HCF** Types	– 0.5 to + 20 – 0.5 to + 18	V V
V_i	Input Voltage	– 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	– 55 to + 125 – 40 to + 85	°C °C
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : **HCC** Types **HCF** Types	3 to 18 3 to 15	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	– 55 to + 125 – 40 to + 85	°C °C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25 °C Min.	25 °C Typ.	25 °C Max.	T_{High}* Min.	T_{High}* Max.	Unit
I_L	Quiescent Current	HCC Types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		HCF Types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output High Voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	

* T_{Low} = – 55°C for **HCC** device : – 40°C for **HCF** device.
* T_{High} = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V min. with V_{DD} = 15V.

STATIC ELECTRICAL CHARACTERISTICS (continued)

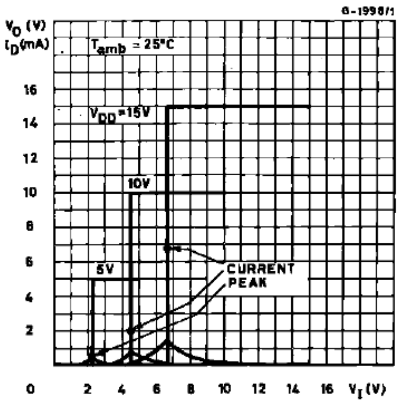
Symbol	Parameter		Test Conditions				Value							Unit
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25 °C Min.	25 °C Typ.	25 °C Max.	T_{High}* Min.	T_{High}* Max.	
V_{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current	HCC Types	0/ 5	2.5		5	– 2		– 1.6	– 3.2		– 1.15		mA
			0/ 5	4.6		5	– 0.64		– 0.51	– 1		– 0.36		
			0/10	9.5		10	– 1.6		– 1.3	– 2.6		– 0.9		
			0/15	13.5		15	– 4.2		– 3.4	– 6.8		– 2.4		
		HCF Types	0/ 5	2.5		5	– 1.53		– 1.36	– 3.2		– 1.1		
			0/ 5	4.6		5	– 0.52		– 0.44	– 1		– 0.36		
			0/10	9.5		10	– 1.3		– 1.1	– 2.6		– 0.9		
			0/15	13.5		15	– 3.6		– 3.0	– 6.8		– 2.4		
I_{OL}	Output Sink Current	HCC Types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	HCC Types	0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
		HCF Types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
C_I	Input Capacitance			Any Input						5	7.5			pF

* T_{Low} = – 55°C for **HCC** device : – 40°C for **HCF** device.
* T_{High} = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V min. with V_{DD} = 15V.

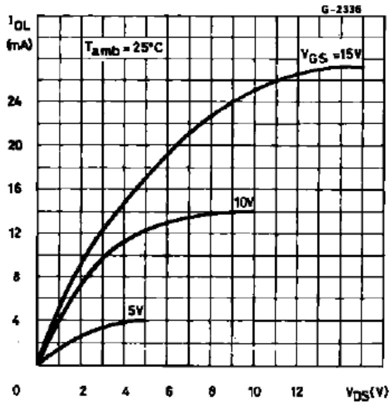
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20ns, R_L = 200kΩ)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay Time		5		125	250	ns
			10		60	125	
			15		45	90	
t_{TLH}, t_{THL}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	

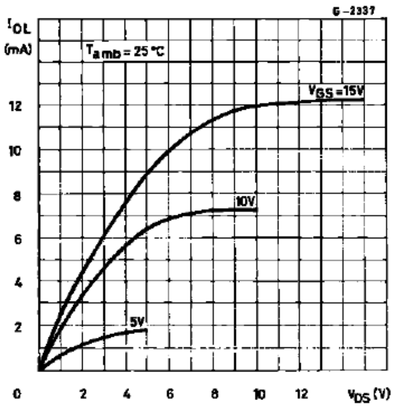
Typical Voltage and Current Transfer Characteristics.



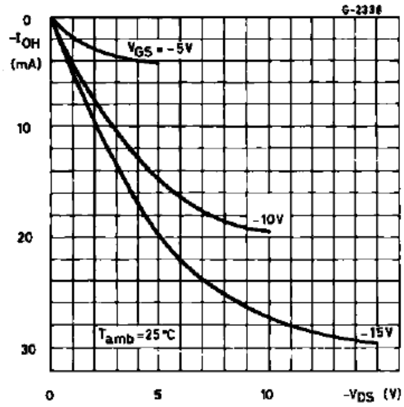
Typical Output Low (sink) Current .



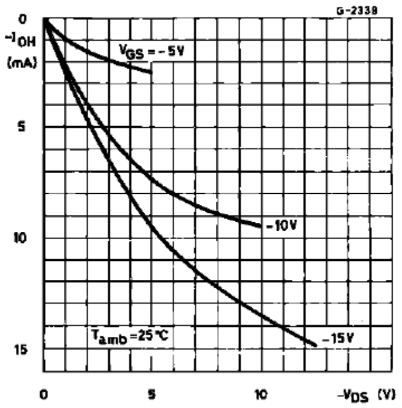
Minimum Output Low (sink) Current Characteristics.



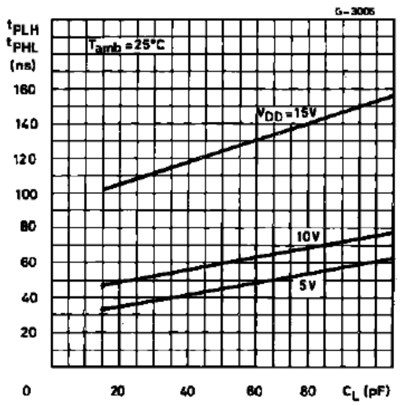
Typical Output High (source) Current Characteristics.



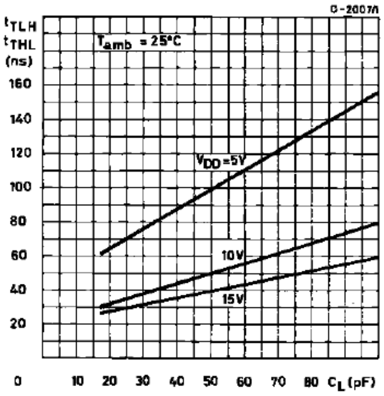
Minimum Output High (source) Current Characteristics.



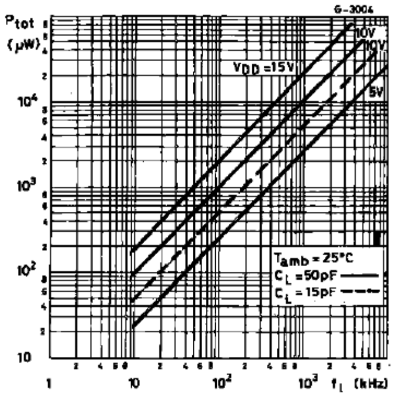
Typical Propagation Delay Time vs. Load Capacitance.



Typical Transition Time vs. Load Capacitance.

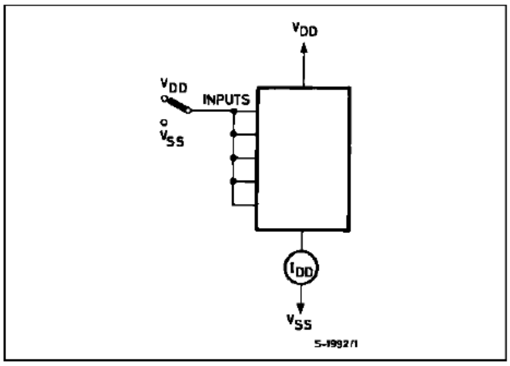


Typical Dynamic Power Dissipation per Gate vs. Frequency.

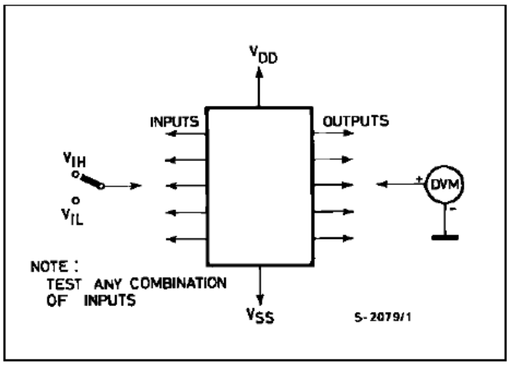


TEST CIRCUITS

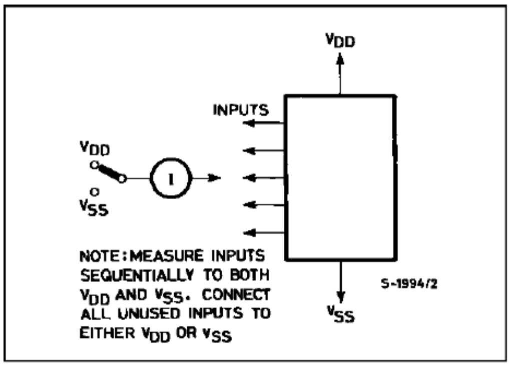
Quiescent Device Current.



Input Voltage.

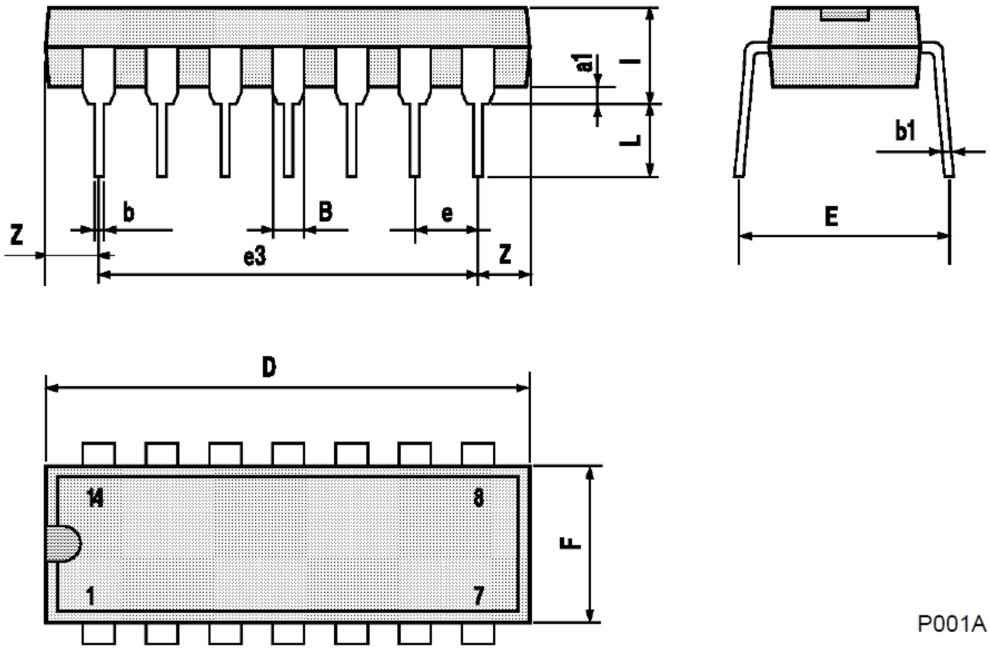


Input Leakage Current.



Plastic DIP14 MECHANICAL DATA

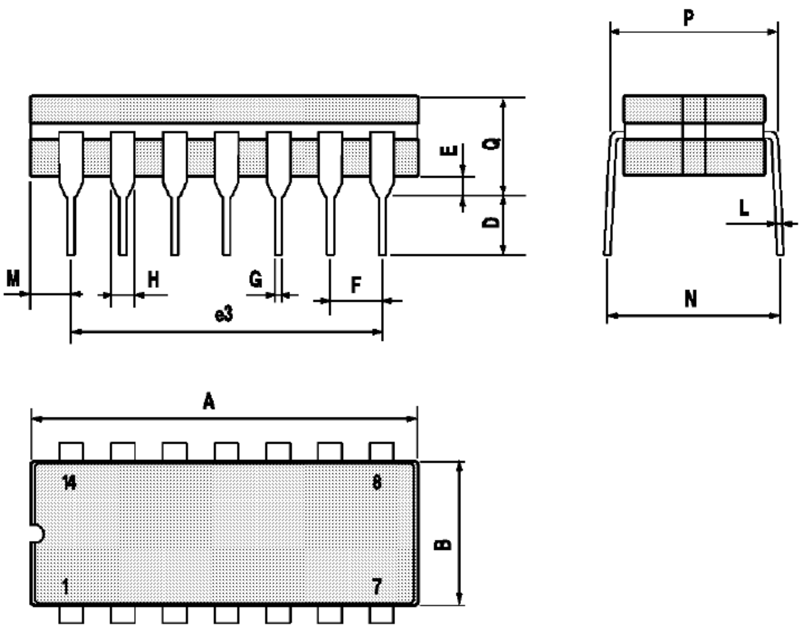
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

Ceramic DIP14/1 MECHANICAL DATA

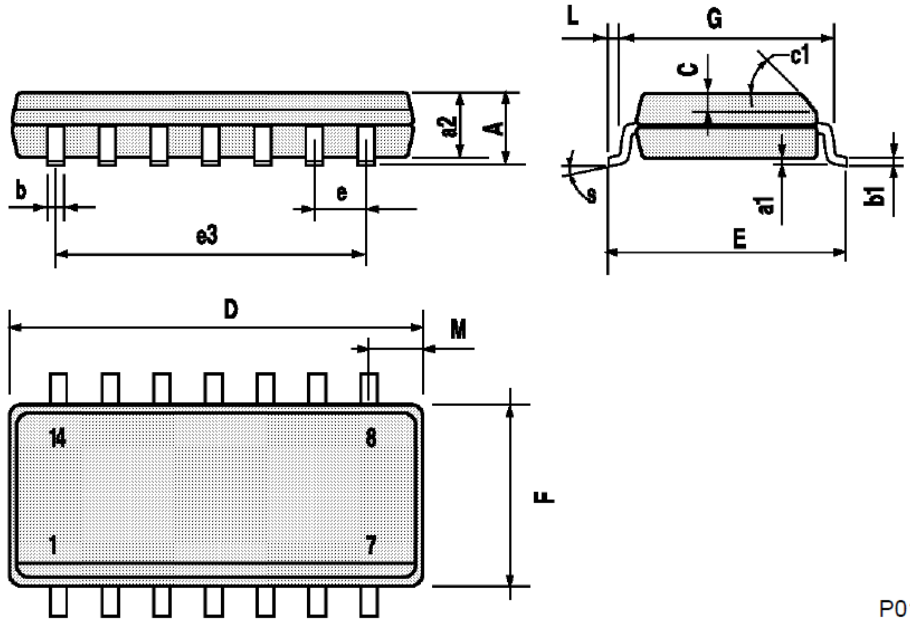
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7.0			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		15.24			0.600	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.54	0.060		0.100
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



P053C

SO14 MECHANICAL DATA

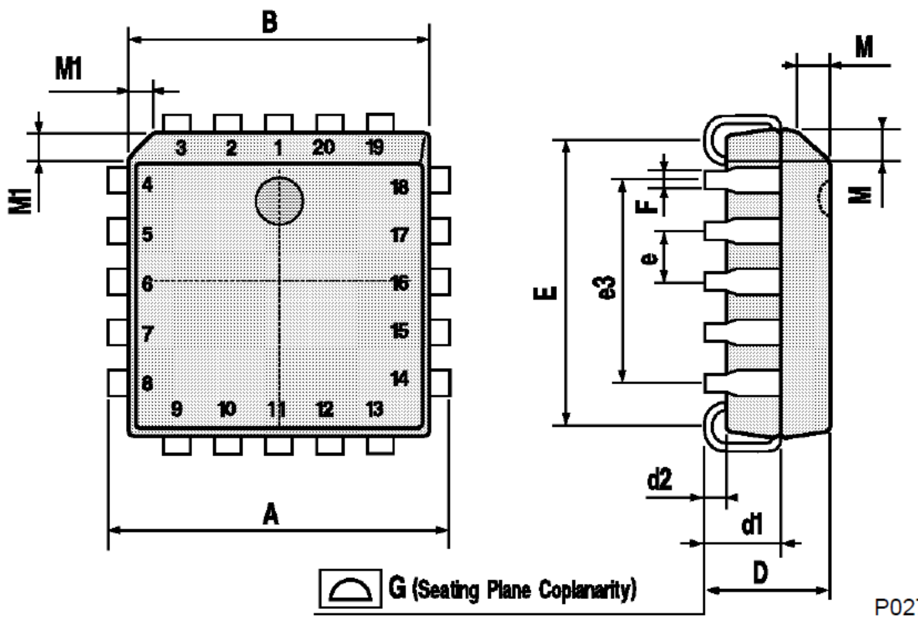
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



P013G

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	

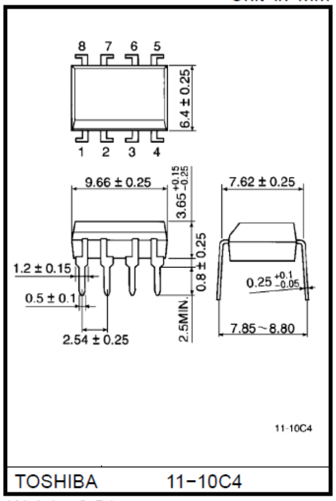


P027A

TLP250

Transistor Inverter
Inverter For Air Conditionor
IGBT Gate Drive
Power MOS FET Gate Drive

Unit in mm



Weight: 0.54 g

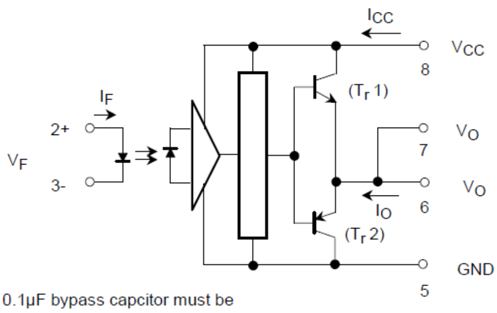
The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and a integrated photodetector.
This unit is 8−lead DIP package.
TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input threshold current: I_F=5mA(max.)
- Supply current (I_{CC}): 11mA(max.)
- Supply voltage (V_{CC}): 10−35V
- Output current (I_O): ±1.5A (max.)
- Switching time (t_{pLH}/t_{pHL}): 1.5μs(max.)
- Isolation voltage: 2500V_{rms}(min.)
- UL recognized: UL1577, file No.E67349
- Option (D4) type
  VDE approved: DIN VDE0884/06.92,certificate No.76823
  Maximum operating insulation voltage: 630V_{PK}
  Highest permissible over voltage: 4000V_{PK}

(Note) When a VDE0884 approved type is needed, please designate the "option (D4)"

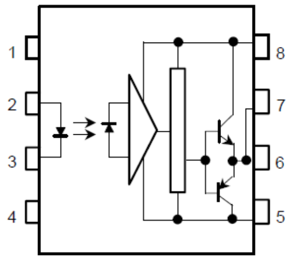
- Creepage distance: 6.4mm(min.)
  Clearance: 6.4mm(min.)

Schmatic



A 0.1μF bypass capcitor must be connected between pin 8 and 5 (See Note 5).

Pin Configuration (top view)



1 : N.C.
2 : Anode
3 : Cathode
4 : N.C.
5 : GND
6 : V_O (Output)
7 : V_O
8 : V_{CC}

Truth Table

		Tr1	Tr2
Input LED	On	On	Off
	Off	Off	On

Absolute Maximum Ratings (Ta = 25°C)

	Characteristic		Symbol	Rating	Unit
LED	Forward current		I_F	20	mA
LED	Forward current derating (Ta ≥ 70°C)		$\Delta I_F / \Delta Ta$	−0.36	mA / °C
LED	Peak transient forward curent	(Note 1)	I_{FPT}	1	A
LED	Reverse voltage		V_R	5	V
LED	Junction temperature		Tj	125	°C
Detector	"H"peak output current (P_W ≤ 2.5μs,f ≤ 15kHz)	(Note 2)	I_{OPH}	−1.5	A
Detector	"L"peak output current (P_W ≤ 2.5μs,f ≤ 15kHz)	(Note 2)	I_{OPL}	+1.5	A
Detector	Output voltage	(Ta ≤ 70°C)	V_O	35	V
Detector	Output voltage	(Ta = 85°C)	V_O	24	V
Detector	Supply voltage	(Ta ≤ 70°C)	V_{CC}	35	V
Detector	Supply voltage	(Ta = 85°C)	V_{CC}	24	V
Detector	Output voltage derating (Ta ≥ 70°C)		$\Delta V_O / \Delta Ta$	−0.73	V / °C
Detector	Supply voltage derating (Ta ≥ 70°C)		$\Delta V_{CC} / \Delta Ta$	−0.73	V / °C
Detector	Junction temperature		Tj	125	°C
Operating frequency		(Note 3)	f	25	kHz
Operating temperature range			T_{opr}	−20~85	°C
Storage temperature range			T_{stg}	−55~125	°C
Lead soldering temperature (10 s)			T_{sol}	260	°C
Isolation voltage (AC, 1 min., R.H.≤ 60%)		(Note 4)	BV_S	2500	Vrms

(Note 1) Pulse width P_W ≤ 1μs, 300pps

(Note 2) Exporenential wavefom

(Note 3) Exporenential wavefom, I_{OPH} ≤ −1.0A(≤ 2.5μs), I_{OPL} ≤ +1.0A(≤ 2.5μs)

(Note 4) Device considerd a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

(Note 5) A ceramic capacitor(0.1μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching propary. The total lead length between capacitor and coupler should not exceed 1cm.

Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.		Unit
Input current, on	$I_{F(ON)}$	7	8	10		mA
Input voltage, off	$V_{F(OFF)}$	0	—	0.8		V
Supply voltage	V_{CC}	15	—	30	20	V
Peak output current	I_{OPH}/I_{OPL}	—	—	±0.5		A
Operating temperature	T_{opr}	−20	25	70	85	°C

Electrical Characteristics (Ta = –20~70°C, unless otherwise specified)

Characteristic		Symbol	Test Circuit	Test Condition	Min.	Typ.*	Max.	Unit
Input forward voltage		V_F	—	I_F = 10 mA , Ta = 25°C		1.6	1.8	V
Temperature coefficient of forward voltage		$\Delta V_F / \Delta Ta$	—	I_F = 10 mA	—	–2.0	—	mV / °C
Input reverse current		I_R	—	V_R = 5V, Ta = 25°C		—	10	μA
Input capacitance		C_T	—	V = 0 , f = 1MHz , Ta = 25°C	—	45	250	pF
Output current	"H" level	I_{OPH}	3	V_{CC} = 30V (*1), I_F = 10 mA, $V_{8\text{-}6}$ = 4V	–0.5	–1.5	—	A
	"L" level	I_{OPL}	2	V_{CC} = 30V (*1), I_F = 0, $V_{6\text{-}5}$ = 2.5V	0.5	2	—	
Output voltage	"H" level	V_{OH}	4	V_{CC1} = +15V, V_{EE1} = –15V, R_L = 200Ω, I_F = 5mA	11	12.8	—	V
	"L" level	V_{OL}	5	V_{CC1} = +15V, V_{EE1} = –15V, R_L = 200Ω, V_F = 0.8V	—	–14.2	–12.5	
Supply current	"H" level	I_{CCH}	—	V_{CC} = 30V, I_F = 10mA, Ta = 25°C	—	7	—	mA
				V_{CC} = 30V, I_F = 10mA	—	—	11	
	"L" level	I_{CCL}	—	V_{CC} = 30V, I_F = 0mA, Ta = 25°C	—	7.5	—	
				V_{CC} = 30V, I_F = 0mA	—	—	11	
Threshold input current	"Output L→H"	I_{FLH}	—	V_{CC1} = +15V, V_{EE1} = –15V, R_L = 200Ω, V_O > 0V	—	1.2	5	mA
Threshold input voltage	"Output H→L"	I_{FHL}	—	V_{CC1} = +15V, V_{EE1} = –15V, R_L = 200Ω, V_O < 0V	0.8	—	—	V
Supply voltage		V_{CC}	—		10	—	35	V
Capacitance (input–output)		C_S	—	V_S = 0 , f = 1MHz, Ta = 25°C	—	1.0	2.0	pF
Resistance(input–output)		R_S	—	V_S = 500V , Ta = 25°C, R.H.≤ 60%	1×10^{12}	10^{14}	—	Ω

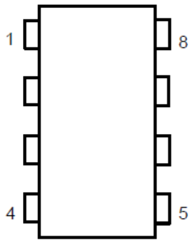
* All typical values are at Ta = 25°C (*1): Duration of I_O time ≤ 50μs

Switching Characteristics (Ta = –20~70°C , unless otherwise specified)

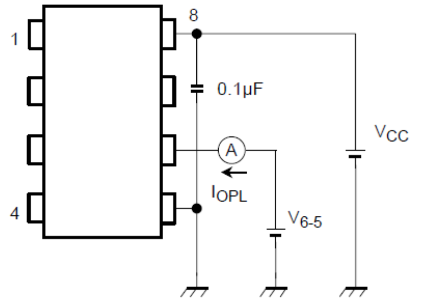
Characteristic		Symbol	Test Circuit	Test Condition	Min.	Typ.*	Max.	Unit
Propagation delay time	L→H	t_{pLH}	6	I_F = 8mA, V_{CC1} = +15V, V_{EE1} = –15V, R_L = 200Ω	—	0.15	0.5	μs
	H→L	t_{pHL}			—	0.15	0.5	
Output rise time		t_r			—	—	—	
Output fall time		t_f			—	—	—	
Common mode transient immunity at high level output		C_{MH}	7	V_{CM} = 600V, I_F = 8mA, V_{CC} = 30V, Ta = 25°C	–5000	—	—	V / μs
Common mode transient immunity at low level output		C_{ML}	7	V_{CM} = 600V, I_F = 0mA, V_{CC} = 30V, Ta = 25°C	5000	—	—	V / μs

* All typical values are at Ta = 25°C

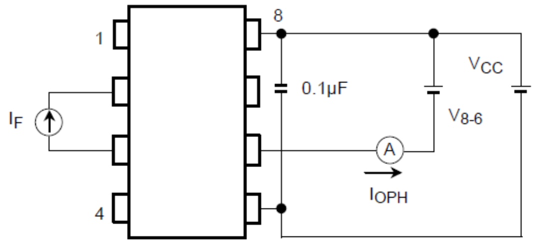
Test Circuit 1 :



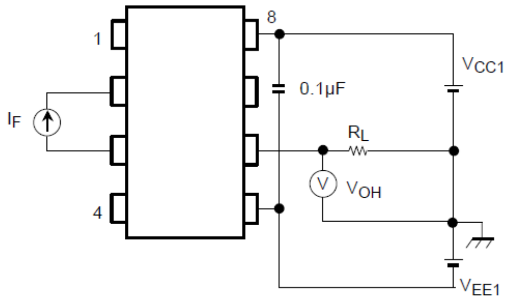
Test Circuit 2 : IOPL



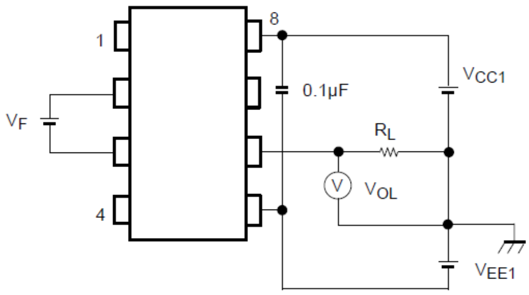
Test Circuit 3 : IOPH



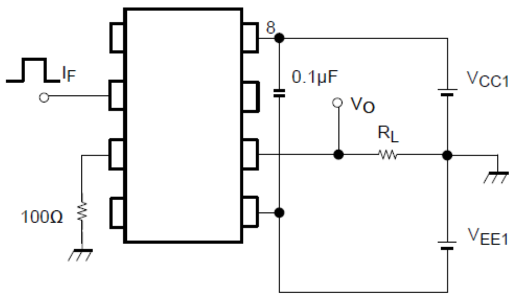
Test Circuit 4 : VOH

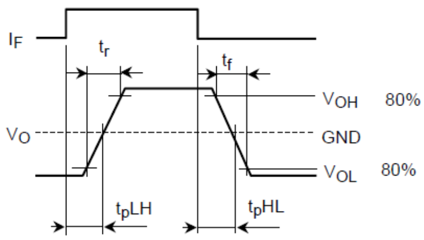


Test Circuit 5 : V_{OL}

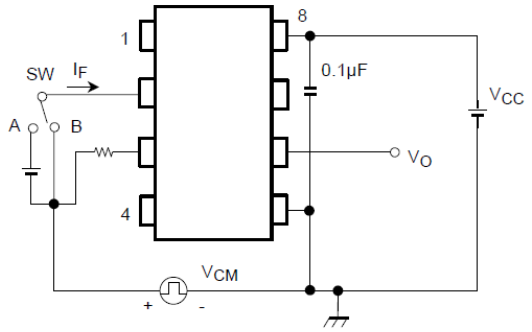


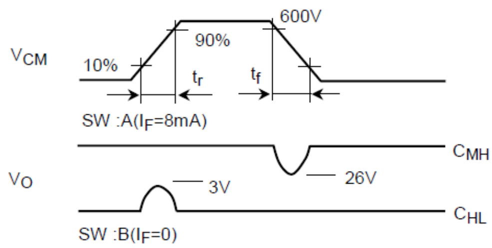
Test Circuit 6: t_{pLH}, t_{pHL}, t_r t_f





Test Circuit 7: C_{MH}, C_{ML}

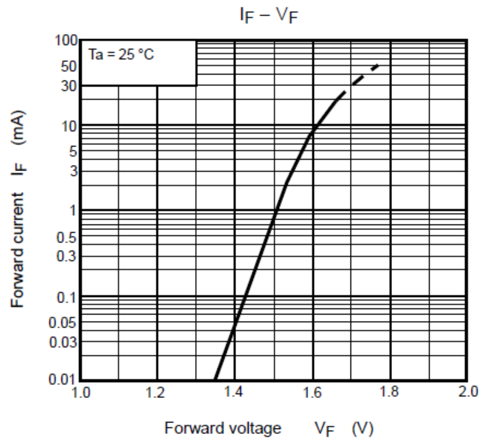


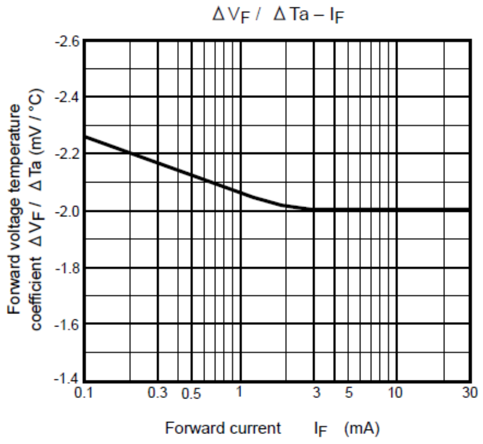


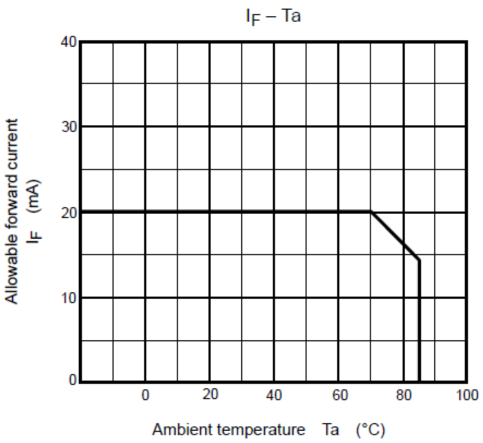
$$C_{ML} = \frac{480\ (V)}{t_{r\ (\mu s)}}$$

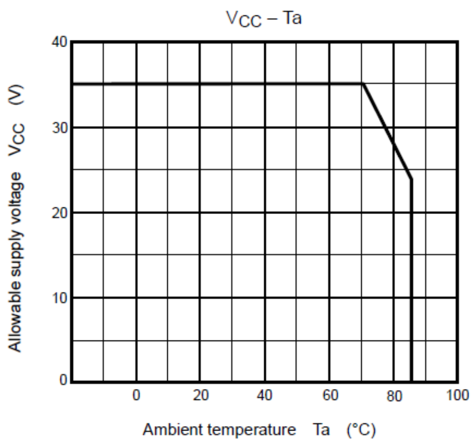
$$C_{MH} = \frac{480\ (V)}{t_{f\ (\mu s)}}$$

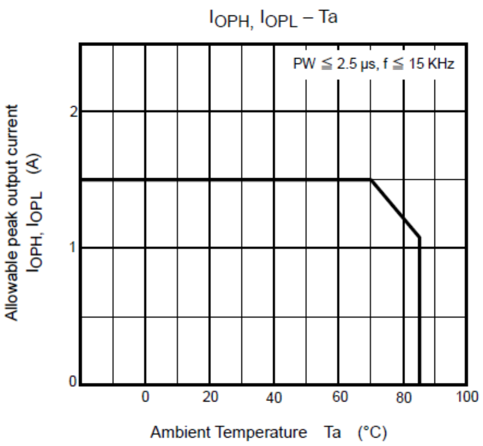
C_{ML}(C_{MH}) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.


I_F – V_F
Ta = 25 °C
Forward current I_F (mA)
100
50
30
10
5
3
1
0.5
0.3
0.1
0.05
0.03
0.01
1.0
1.2
1.4
1.6
1.8
2.0
Forward voltage V_F (V)


ΔV_F / ΔTa – I_F
Forward voltage temperature coefficient ΔV_F / ΔTa (mV / °C)
-2.6
-2.4
-2.2
-2.0
-1.8
-1.6
-1.4
0.1
0.3
0.5
1
3
5
10
30
Forward current I_F (mA)


I_F – Ta
Allowable forward current I_F (mA)
40
30
20
10
0
0
20
40
60
80
100
Ambient temperature Ta (°C)


V_{CC} – Ta
Allowable supply voltage V_{CC} (V)
40
30
20
10
0
0
20
40
60
80
100
Ambient temperature Ta (°C)


I_{OPH}, I_{OPL} – Ta
PW ≦ 2.5 μs, f ≦ 15 KHz
Allowable peak output current I_{OPH}, I_{OPL} (A)
2
1
0
0
20
40
60
80
100
Ambient Temperature Ta (°C)

MUR1510, MUR1515, MUR1520, MUR1540, MUR1560

Preferred Devices

SWITCHMODE™ Power Rectifiers

These state−of−the−art devices are a series designed for use in switching power supplies, inverters and as free wheeling diodes.

Features

- Ultrafast 35 and 60 Nanosecond Recovery Time
- 175°C Operating Junction Temperature
- Popular TO−220 Package
- High Voltage Capability to 600 V
- Low Forward Drop
- Low Leakage Specified @ 150°C Case Temperature
- Current Derating Specified @ Both Case and Ambient Temperatures
- Pb−Free Packages are Available*

Mechanical Characteristics:

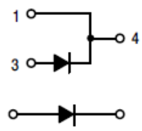
- Case: Epoxy, Molded
- Weight: 1.9 Grams (Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead Temperature for Soldering Purposes: 260°C Max. for 10 Seconds

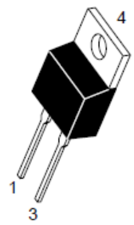
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

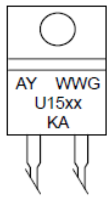
ULTRAFAST RECTIFIERS
15 AMPERES, 100−600 VOLTS





TO−220AC
CASE 221B
PLASTIC

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package
U15xx	= Device Code xx = 10, 15, 20, 40 or 60
KA	= Diode Polarity

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

MAXIMUM RATINGS

Rating	Symbol	MUR 1510	1515	1520	1540	1560	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	100	150	200	400	600	V
Average Rectified Forward Current (Rated V_R)	$I_{F(AV)}$	15 @ T_C = 150°C				15 @ T_C = 145°C	A
Peak Rectified Forward Current (Rated V_R, Square Wave, 20 kHz)	I_{FRM}	30 @ T_C = 150°C				30 @ T_C = 145°C	A
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions halfwave, single phase, 60 Hz)	I_{FSM}	200			150		A
Operating Junction Temperature and Storage Temperature Range	T_J, T_{stg}	−65 to +175					°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Maximum Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.5	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	1520	1540	1560	Unit
Maximum Instantaneous Forward Voltage (Note 1) (i_F = 15 A, T_C = 150°C) (i_F = 15 A, T_C = 25°C)	v_F	 0.85 1.05	 1.12 1.25	 1.20 1.50	V
Maximum Instantaneous Reverse Current (Note 1) (Rated DC Voltage, T_C = 150°C) (Rated DC Voltage, T_C = 25°C)	i_R	 500 10	 500 10	 1000 10	μA
Maximum Reverse Recovery Time (I_F = 1.0 A, di/dt = 50 A/μs)	t_{rr}	35	60		ns

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

MUR1510, MUR1515, MUR1520

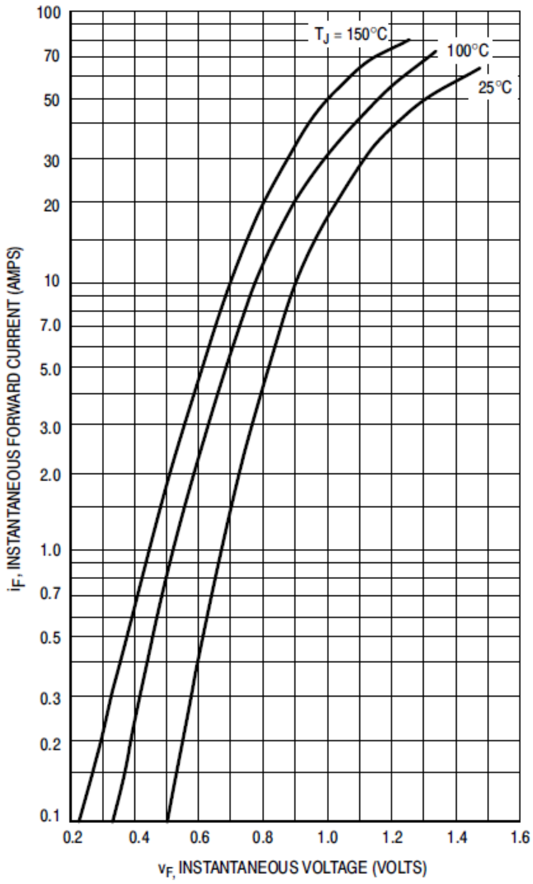


Figure 1. Typical Forward Voltage

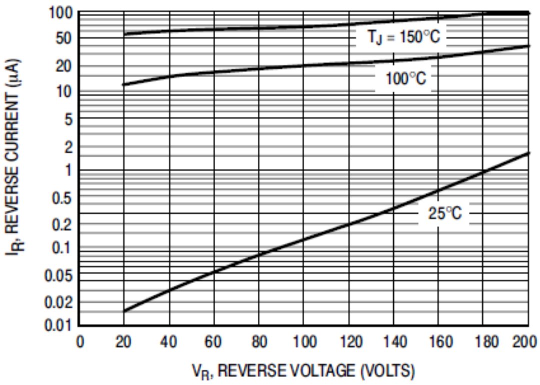


Figure 2. Typical Reverse Current

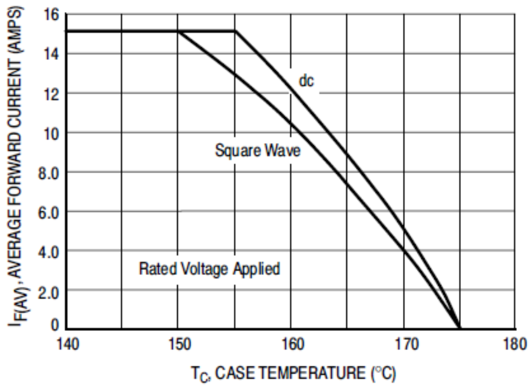


Figure 3. Current Derating, Case

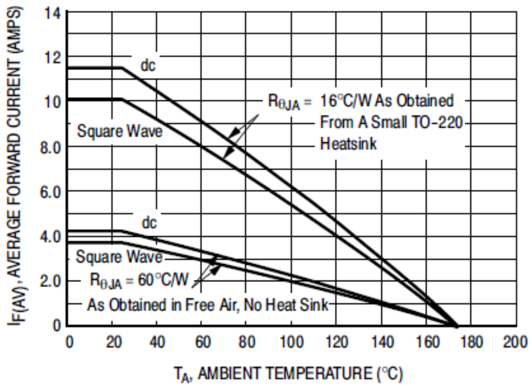


Figure 4. Current Derating, Ambient

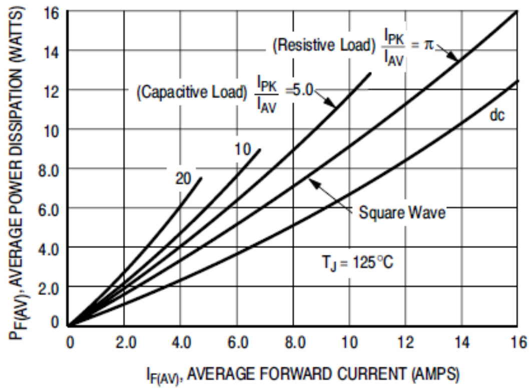


Figure 5. Power Dissipation

MUR1540

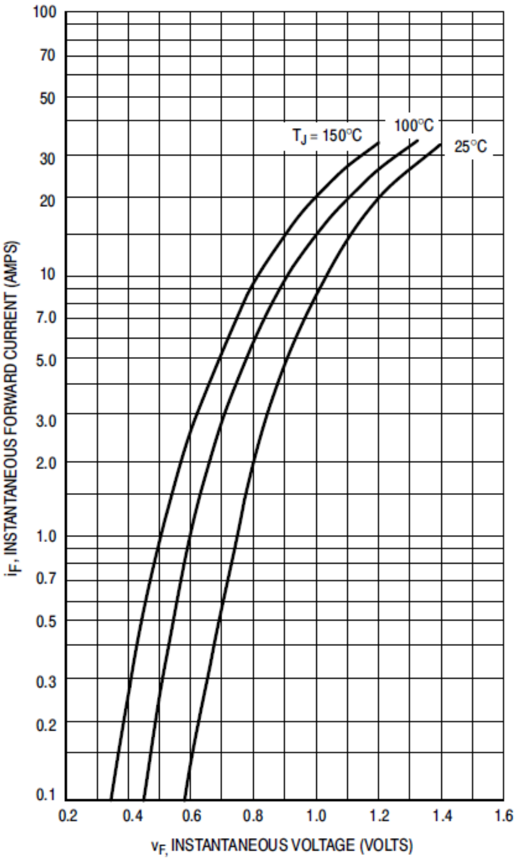


Figure 6. Typical Forward Voltage

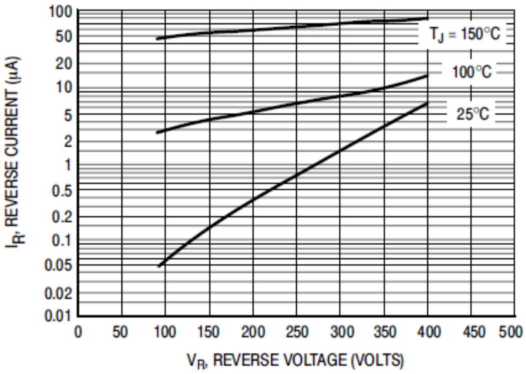


Figure 7. Typical Reverse Current

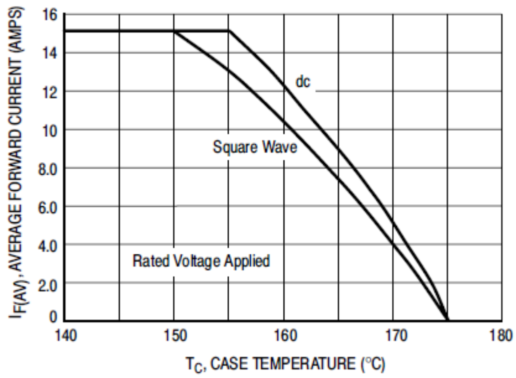


Figure 8. Current Derating, Case

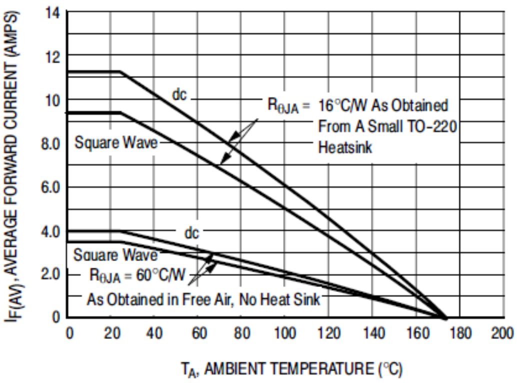


Figure 9. Current Derating, Ambient

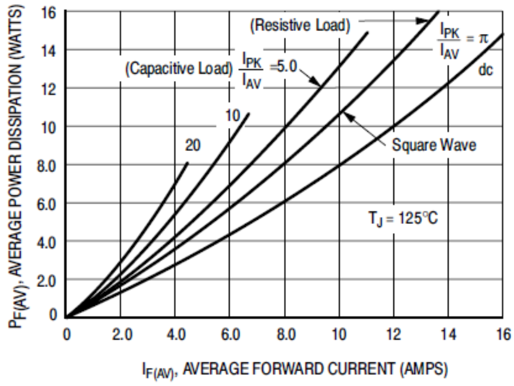


Figure 10. Power Dissipation

MUR1560

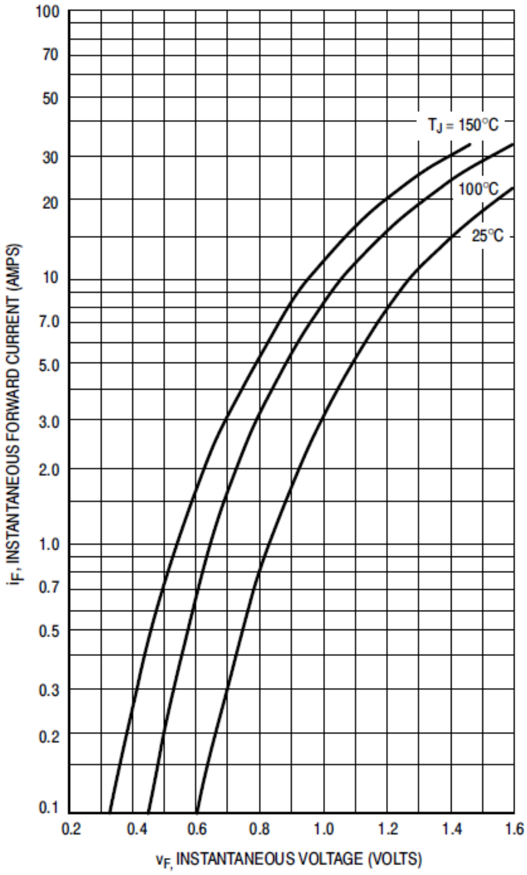


Figure 11. Typical Forward Voltage

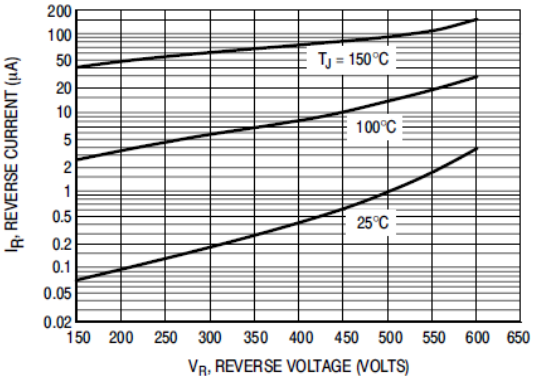


Figure 12. Typical Reverse Current

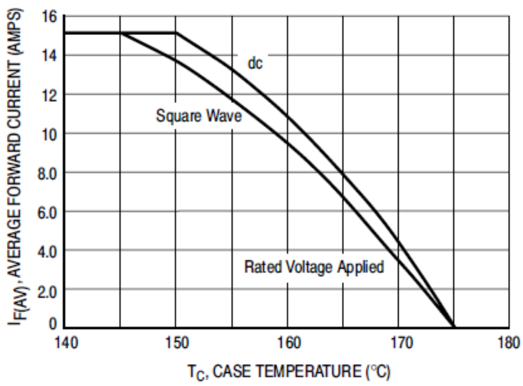


Figure 13. Current Derating, Case

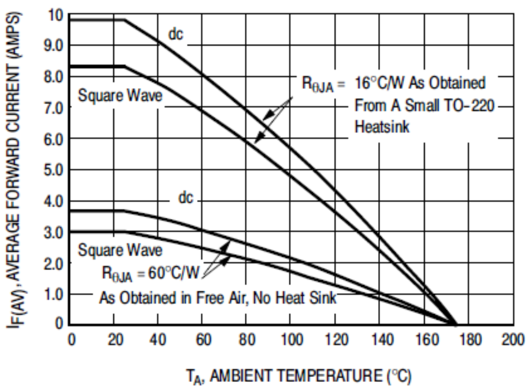


Figure 14. Current Derating, Ambient

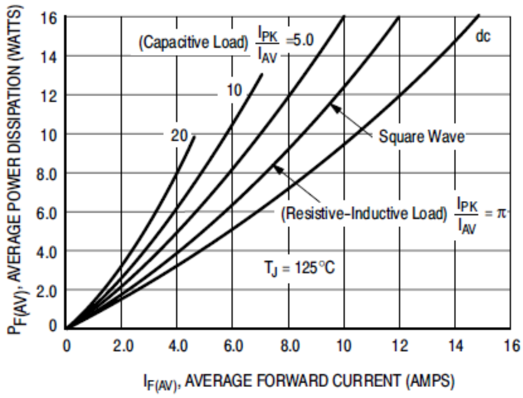


Figure 15. Power Dissipation

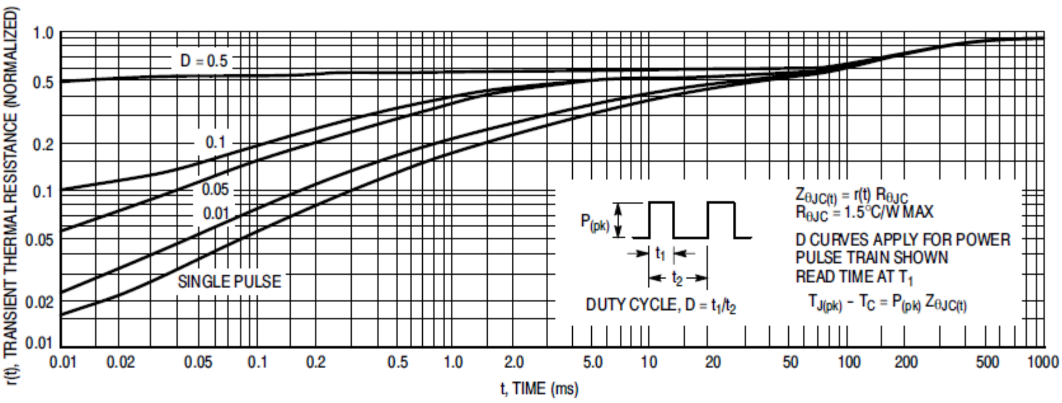


Figure 16. Thermal Response

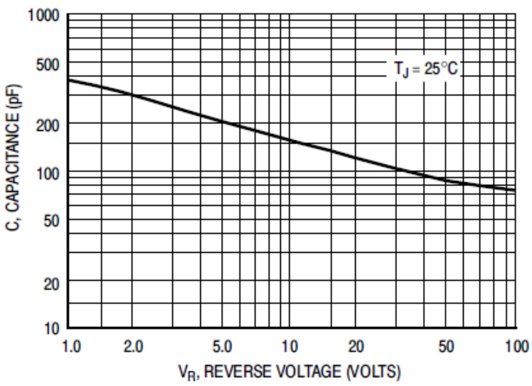


Figure 17. Typical Capacitance

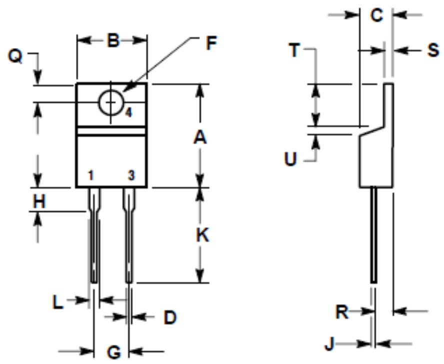
ORDERING INFORMATION

Device	Package	Shipping†
MUR1510	TO−220	50 Units / Rail
MUR1510G	TO−220 (Pb−Free)	
MUR1515	TO−220	
MUR1515G	TO−220 (Pb−Free)	
MUR1520	TO−220	
MUR1520G	TO−220 (Pb−Free)	
MUR1540	TO−220	
MUR1540G	TO−220 (Pb−Free)	
MUR1560	TO−220	
MUR1560G	TO−220 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TO−220 TWO−LEAD
CASE 221B−04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.595	0.620	15.11	15.75
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.82
D	0.025	0.035	0.64	0.89
F	0.142	0.147	3.61	3.73
G	0.190	0.210	4.83	5.33
H	0.110	0.130	2.79	3.30
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.14	1.39
T	0.235	0.255	5.97	6.48
U	0.000	0.050	0.000	1.27

PD-93991D

International
IOR Rectifier

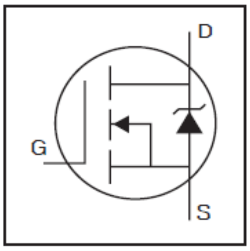
AUTOMOTIVE MOSFET

IRF1405

Typical Applications
- Electric Power Steering (EPS)
- Anti-lock Braking System (ABS)
- Wiper Control
- Climate Control
- Power Door

Benefits
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

HEXFET® Power MOSFET



V_{DSS} = 55V

$R_{DS(on)}$ = 5.3mΩ

I_D = 169A⑥

TO-220AB

Description
Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

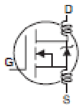
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	169⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	118⑥	
I_{DM}	Pulsed Drain Current ①	680	
P_D @T_C = 25°C	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	560	mJ
I_{AR}	Avalanche Current	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑦		mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

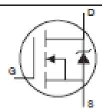
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.057	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	4.6	5.3	mΩ	V_{GS} = 10V, I_D = 101A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = 10V, I_D = 250μA
g_{fs}	Forward Transconductance	69	—	—	S	V_{DS} = 25V, I_D = 110A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	170	260	nC	I_D = 101A
Q_{gs}	Gate-to-Source Charge	—	44	66		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	62	93		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	V_{DD} = 38V
t_r	Rise Time	—	190	—		I_D = 101A
$t_{d(off)}$	Turn-Off Delay Time	—	130	—		R_G = 1.1Ω
t_f	Fall Time	—	110	—		V_{GS} = 10V ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	5480	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1210	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	280	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	5210	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	900	—		V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	—	1500	—		V_{GS} = 0V, V_{DS} = 0V to 44V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	169⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	680		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 101A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	88	130	ns	T_J = 25°C, I_F = 101A
Q_{rr}	Reverse RecoveryCharge	—	250	380	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.11mH R_G = 25Ω, I_{AS} = 101A. (See Figure 12).

③ $I_{SD} \leq$ 101A, di/dt $\leq$ 210A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

④ Pulse width $\leq$ 400μs; duty cycle $\leq$ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

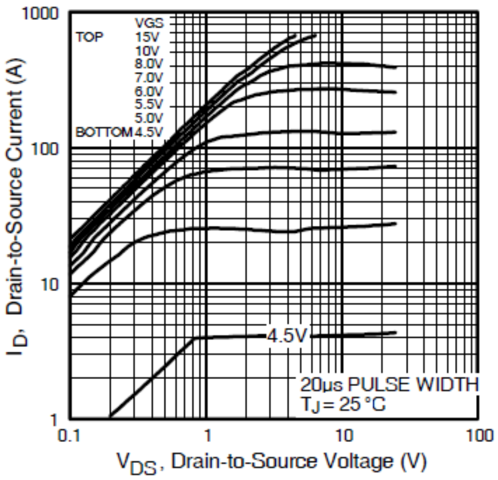


Fig 1. Typical Output Characteristics

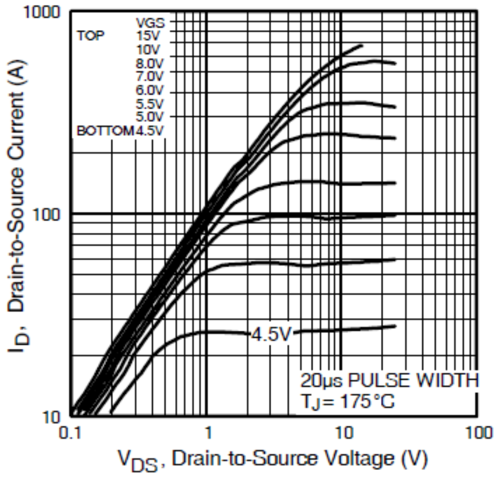


Fig 2. Typical Output Characteristics

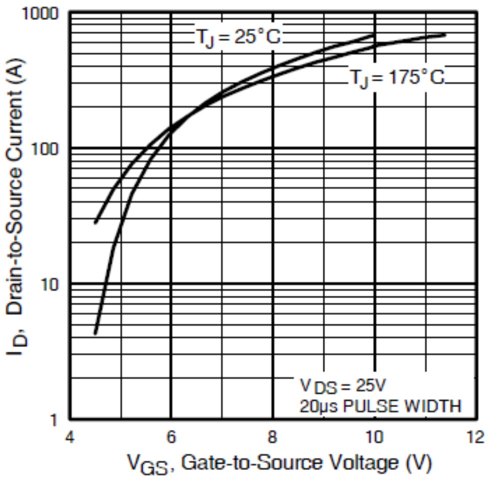


Fig 3. Typical Transfer Characteristics

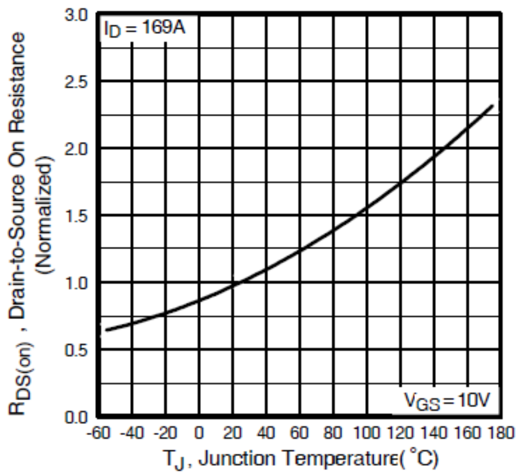


Fig 4. Normalized On-Resistance Vs. Temperature

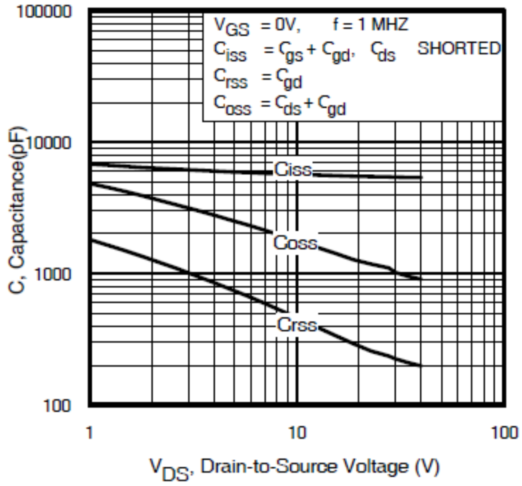


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

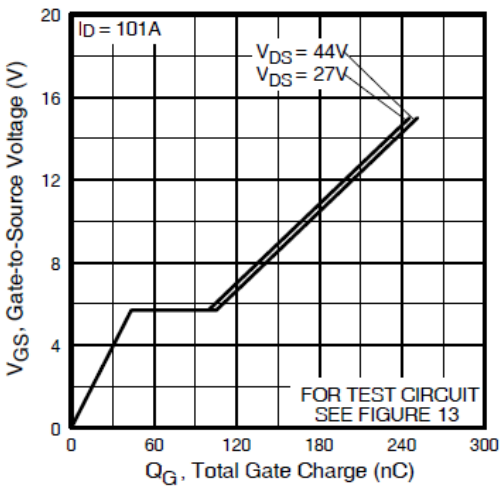


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

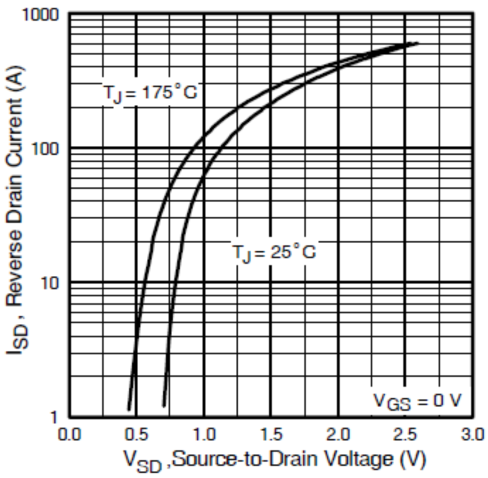


Fig 7. Typical Source-Drain Diode Forward Voltage

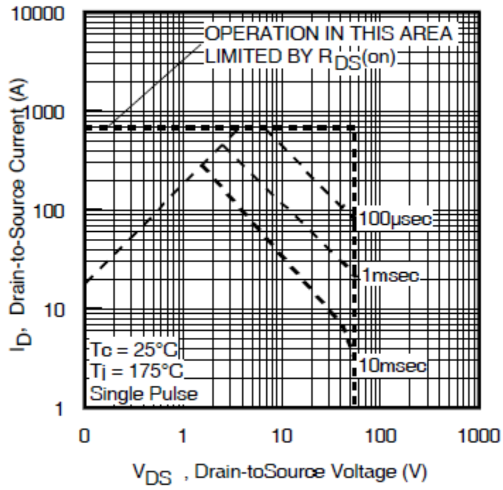


Fig 8. Maximum Safe Operating Area

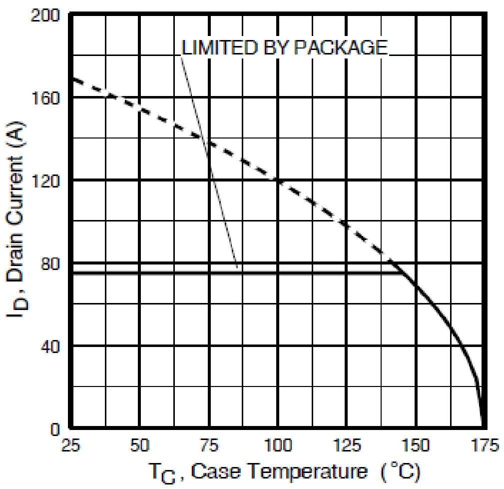


Fig 9. Maximum Drain Current Vs. Case Temperature

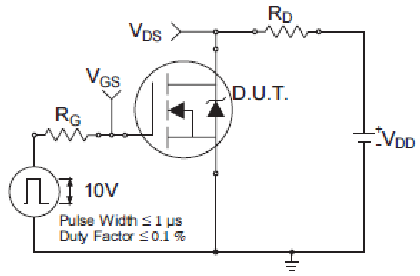


Fig 10a. Switching Time Test Circuit

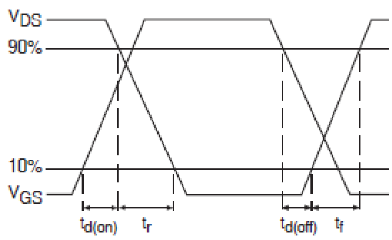


Fig 10b. Switching Time Waveforms

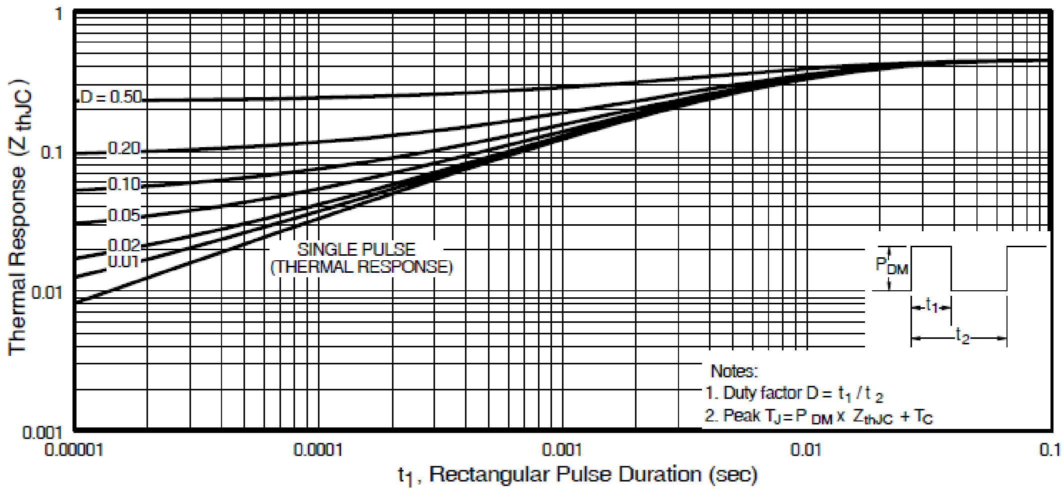


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

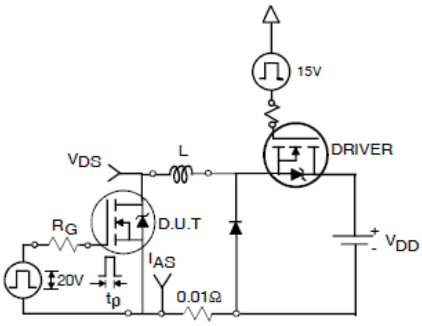


Fig 12a. Unclamped Inductive Test Circuit

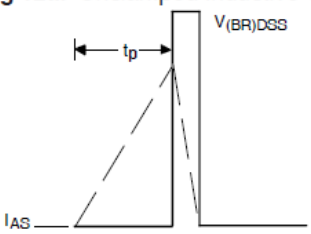


Fig 12b. Unclamped Inductive Waveforms

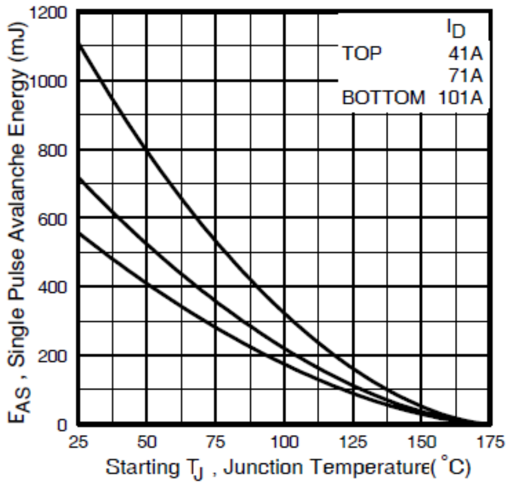


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

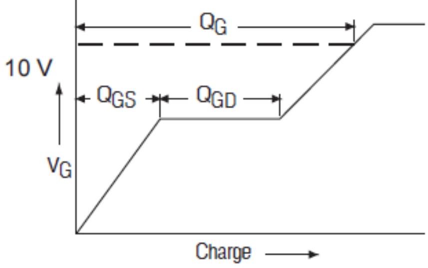


Fig 13a. Basic Gate Charge Waveform

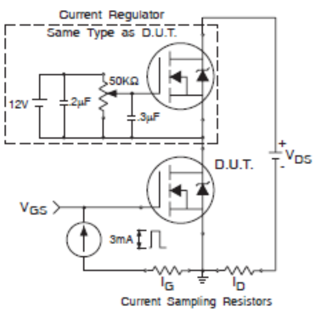


Fig 13b. Gate Charge Test Circuit

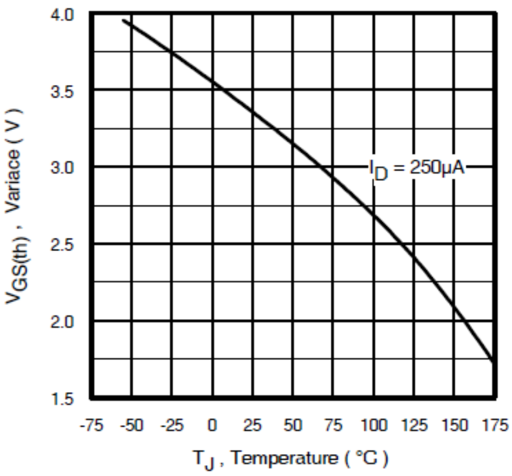


Fig 14. Threshold Voltage Vs. Temperature

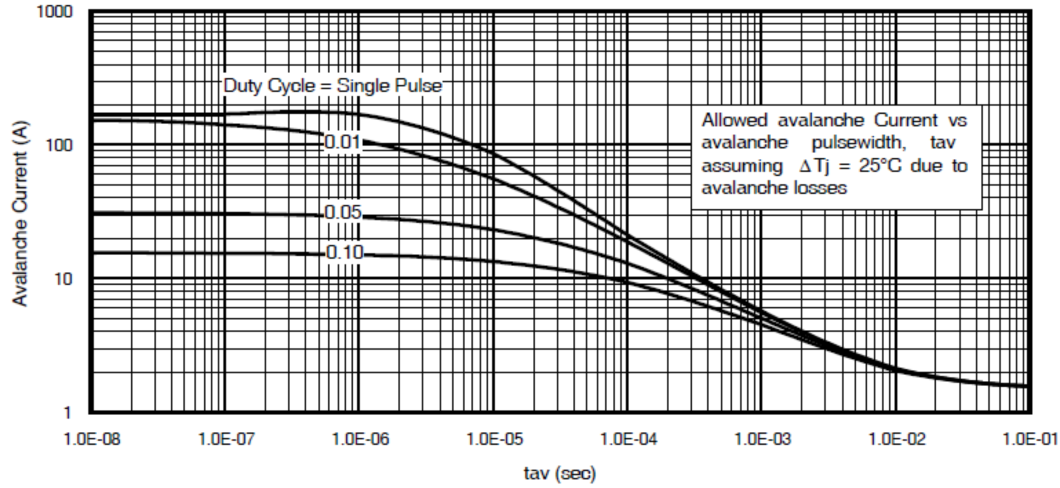


Fig 15. Typical Avalanche Current Vs.Pulsewidth

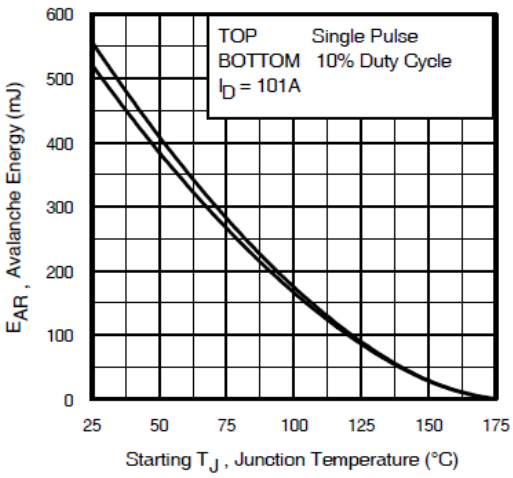


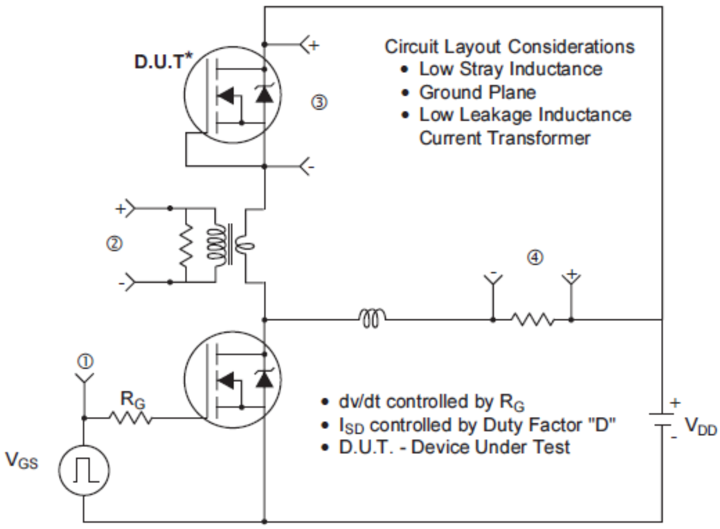
Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

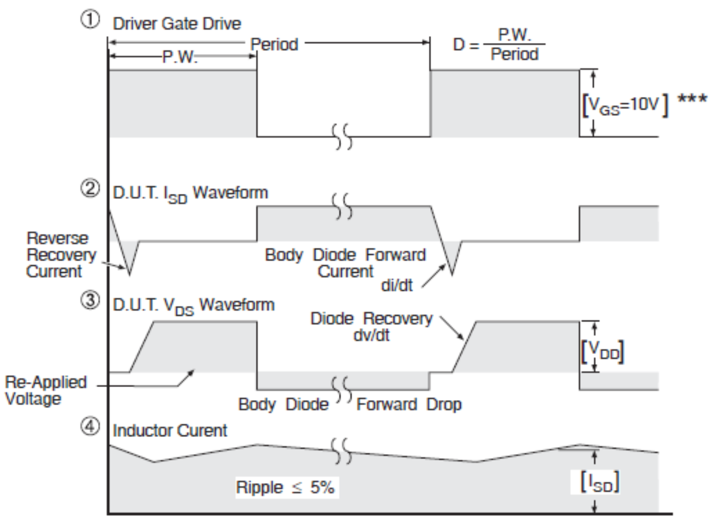
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit



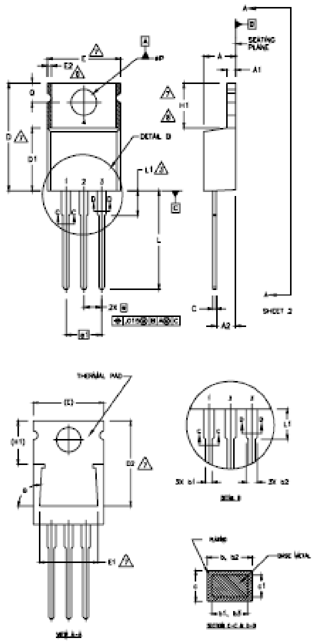
* Reverse Polarity of D.U.T for P-Channel



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5 DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
6 CONTROLLING DIMENSION : INCHES.
7 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8 DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.82	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.96	.015	.038	5
b2	1.15	1.77	.045	.070	
b3	1.15	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	12.19	12.88	.480	.507	7
E	9.66	10.66	.380	.420	4,7
E1	8.38	8.89	.330	.350	7
e	2.54 BSC		.100 BSC		
e1	5.08		.200 BSC		
H1	5.85	6.55	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	-	6.35	-	.250	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	
ø	90°-93°		90°-93°		

LEAD ASSIGNMENTS

HEXFET
1.- GATE
2.- DRAIN
3.- SOURCE

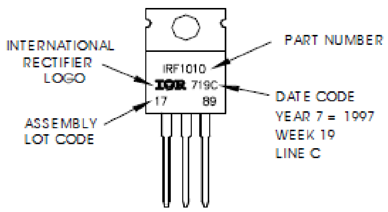
IGBTs, CoPACK
1.- GATE
2.- COLLECTOR
3.- EMITTER

DIODES
1.- ANODE/OPEN
2.- CATHODE
3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



TO-220AB packages are not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International IOR Rectifier

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